UNITED STATES DISTRICT COURT
WESTERN DISTRICT OF TEXAS
WACO DIVISION

PARKERVISION, INC., Plaintiff, vs. INTEL CORPORATION, Defendant.	Civil Action No. 6:20-cv-00562-ADA **JURY TRIAL DEMANDED**

INTEL CORPORATION'S RESPONSIVE CLAIM CONSTRUCTION BRIEF

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I. INTRODUCTION

ParkerVision ("PV") asserts three patents[1] directed to the well-known transceiver-technology concepts of "down-conversion" (the process by which a wireless device shifts a received signal to a lower frequency so the device can process the data sent by the signal) and its inverse, "up-conversion" (the process by which a low-frequency signal is shifted to a higher frequency for transmission). These concepts were well known and had been extensively studied at the time PV filed its patent applications. In an effort to avoid the substantial prior art that already existed in the field—prior art that included many other methods of performing down-conversion and up-conversion—PV was forced to claim very specific techniques for performing these functions that are now described in its patents. Intel's proposed constructions are faithful to this intrinsic evidence. PV's proposed constructions, on the other hand, are untethered from any of the allegedly distinguishing characteristics of the claimed inventions.[2] Intel respectfully requests that the Court construe the terms as Intel has proposed, consistent with the intrinsic evidence and with well-settled principles of patent law.[3]

II. THE '706 PATENT

The '706 patent purports to have invented new methods and apparatuses for ***down-converting*** and ***filtering*** an incoming signal at a receiver "in an ***integrated***, ***unified*** manner."[4] '706, Abstract. The specification describes three basic functions of a receiver: frequency selection (*i.e.*, filtering),

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[1] The patents-in-suit—U.S. Patent Nos. 6,049,706, 7,050,508, and 8,190,108—are attached as Exhibits 1-3 to the M. Lalli Declaration filed concurrently herewith.

[2] Even though PV was obligated to disclose its constructions on November 24, 2020 and the parties had ample time to meet and confer (given that PV delayed the filing of its opening brief by two months), PV modified 11 out of 22 of its proposed constructions for the first time in its opening brief without having disclosed to Intel that it was doing so.

[3] The parties have agreed to rely on their briefing in *ParkerVision, Inc. v. Intel Corp.*, No. 6:20-cv-108 (W.D. Tex.) regarding three terms that are also in dispute in this case: "under-sampling," "storage module," and "switch." Intel does not seek to "re-argue" these terms (Pl. Op. 1-2), but Intel maintains its positions regarding those terms and reserves its right to appeal should the Court adopt the same constructions in this case.

[4] All emphasis in this brief is added unless otherwise noted.

amplification, and frequency translation (*i.e.*, down-conversion). *Id.*, 1:20-3:23. According to the '706 patent, in a conventional receiver, an incoming RF signal passes through a first filter ("Band Select Filter 102") to filter out signals with frequencies outside a wide range of frequencies called a "band." *Id.*, 1:58-67. The filter is followed by a Low-Noise Amplifier ("LNA 104"), and then a mixer, which "operates to down-convert the band-select filtered spectrum 408 in a well-known manner." *Id.*, 1:30-2:8; Fig. 1. The down-converted signal passes through a second filter ("Channel Select Filter 108"), which filters out signals with frequencies other than those in a narrow "channel" containing the desired signal. *Id.*, 2:61-64. The desired frequency is then amplified ("Amplifier 110") and sent downstream for further processing. *Id.*, 2:61-64, 3:3-14.

The patent describes a well-known problem with such conventional receivers: when the desired frequency ("Channel Select Filtered Signal 412") includes a "desired signal component 420" and an undesired, "spurious component 404C" at the same frequency (i.e., "17" in Fig. 4F), both the desired and spurious components will pass through the Channel Select Filter. *Id.*, Fig. 4F, 2:51-3:2. The subsequent amplifier (110) then amplifies both the desired and spurious components, causing "degraded performance." *Id.*, 3:3-23.

To address this problem, the '706 patent proposes performing the filtering and down-conversion operations "in an integrated, unified manner." *Id.*, Abstract; *id.*, 10:31-33 ("According to the present invention, frequency selectivity [filtering] and frequency translation [down-conversion] are performed as a single unified (i.e., integrated) operation."). The '706 patent states that "***[t]he present invention*** is directed to methods and apparatuses for ***unified down-converting and filtering*** (UDF)." *Id.*, 12:14-44. In Figure 26, for example, a UDF module 2622 contains an input filter 1106 (green) that itself contains a down-convert and delay module 2624 (blue).

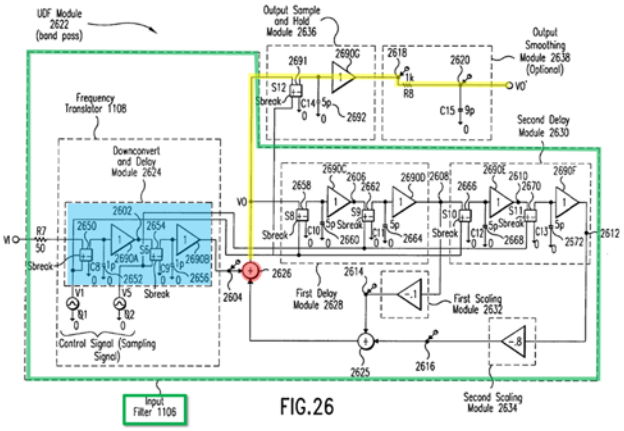


FIG.26

Id., Fig. 26. Filtering typically involves using delayed versions of input and output signals. *Id.*, 7:46-50; Fig. 21; Dr. van der Weide Decl., ¶¶ 57-58 ("VDW"). In Figure 26, the down-convert and delay module 2624 first down-converts an input signal by producing an "input sample" and then delays that input sample for purposes of filtering. *Id.*, 16:15-27; 26:1-30; 28:20-41. Additional delay module(s) (2628, 2630) delay instances of an output signal 1706 (yellow). Adder 2626 (red) adds the delayed input sample and the delayed instances of output signal 1706 to generate output signal 1706. *Id.*, 16:13-41; 28:20-41; VDW ¶ 58.

The patent asserts that the combination of the delayed instances of the output signal filters out unwanted components of the signal, leaving the desired output signal. *Id.*, 24:48-60; VDW ¶ 58.

A. Down Convert and Delay Terms

Claim Term	Proposed Constructions
"a down-convert and delay module to under-sample an input signal to produce an input sample of a down-converted image of said input signal, and to delay said input sample" ('706 patent, claims 1, 7)	**Intel:** **Function**: under-sample an input signal to produce an input sample of a down-converted image of said input signal, and to delay said input sample **Structure**: the down convert and delay module 2624 in Fig. 26 and described at 26:1-27:21 and 28:20-41, that includes the switches 2650 and 2654, and the capacitors 2652 and 2656; and equivalents thereof **PV**: Plain and ordinary meaning
"a frequency translator to produce a sample of a down-converted image	**Intel:** **Function**: produce a sample of a down-converted image of an input signal, and to delay said sample

Claim Term	Proposed Constructions
of an input signal, and to delay said sample" ('706 patent, claim 34)	**Structure**: the down convert and delay module 2624 in Fig. 26 and described at 26:1-27:21 and 28:20-41, that includes the switches 2650 and 2654, and the capacitors 2652 and 2656; and equivalents thereof. **PV**: Plain and ordinary meaning

The parties dispute whether these terms are means-plus-function (as Intel contends) or whether they connote definite structure to allow a "plain and ordinary meaning" construction (as PV contends).

Intel's Proposal. Section 112 ¶ 6 creates a bargain for a patentee: "In exchange for being able to draft a claim limitation in purely functional language … the functional claim language covers only 'the corresponding structure, material, or acts *described* in the specification and equivalents thereof.'" *Noah Sys., Inc. v. Intuit Inc.*, 675 F.3d 1302, 1318 (Fed. Cir. 2012). A claim term must be construed as means-plus-function if it "recites 'function without reciting sufficient structure for performing that function,'" even if the claim does not include the phrase "means for." *Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1349 (Fed. Cir. 2015).

The disputed limitations recite either a "down-convert and delay module" or a "frequency translator" that is used to under-sample (or sample) an input signal and delay the sample. Neither term connotes sufficient, definite structure to perform the claimed functions. "Module" is a "well-known nonce word that can operate as a substitute for 'means' in the context of § 112, para. 6." *Williamson*, 792 F.3d at 1350 ("***Module' …does not provide any indication of structure*** because it sets forth the same black box recitation of structure for providing the same specified function ***as if the term 'means' had been used***."). "[D]own-convert and delay module" is not a term known to skilled artisans, VDW ¶¶ 60-61, and just as in *Williamson*, the prefix "down-convert and delay" simply describes what a generic "module" ***does***—it down-converts and delays—and "does not impart structure into the term 'module.'" *Id.* at 1351. Similarly, the term "frequency translator" fails to connote sufficient structure—instead it connotes the function of translating a frequency. The patent refers to the frequency translator

in functional terms, not as a purportedly well-known structure to persons of ordinary skill in the art. '706, 13:44-46 ("The frequency translator 1108 conceptually represents that portion of the UDF module 1102 that performs frequency translation (down conversion)."); VDW ¶¶ 67-68. The terms therefore must be construed as means-plus-function. *Williamson*, 792 F.3d at 1349.

Intel's proposed construction properly sets forth the structure disclosed for performing the claimed function.[5] The specification clearly links both the "down-convert and delay module" and the "frequency translator" terms to the "Downconvert and Delay Module 2624" and the "Frequency Translator 1108" in Figure 26—which are essentially coextensive. As discussed in detail regarding the "first delaying means" limitation, the first switch (2650) and capacitor (2652) in the "Downconvert and Delay Module 2624" under-sample the input signal to down-convert it, and the second switch (2654) and capacitor (2656) delay the input sample. '706, 28:24-28, 26:5-8; 26:25-30.

PV criticizes Intel's proposed construction for not including structures from Figures 17, 19, 23, 53A, and 53A-1. Pl. Op. 9 n.4. But none of those figures disclose structure for performing the complete claimed function—under-sampling and delay. The "down-convert and delay modules" 1708, 1908, and 2308 in Figures 17, 19, and 23 are all empty "black boxes" that fail to disclose any structure for performing the claimed function. *Williamson*, 792 F.3d at 1350 ("[T]he word 'module' does not provide any indication of structure because it sets forth the same black box recitation of structure for providing the same specified function as if the term 'means' had been used."). The "aliasing modules"

[5] PV's only criticism of Intel's proposed function is that it does not include language from the last limitations of claims 1, 7, and 34, i.e., "under-sampl[ing] said input signal according to a control signal." Pl. Op. 9 n.4, 33 n.17. Intel has no objection to including that language.

in Figures 53A and 53A-1 simply down-convert, but do not delay. *Infra,* II.G.[6]

PV's Proposal. PV's "plain and ordinary meaning" proposed construction should be rejected for at least two reasons. ***First,*** PV is wrong that a "down-convert and delay module" "has a known structure that incorporates components/circuits such as a switch … and a capacitor/storage element." PV's only support is one sentence from the specification: "The downconvert and delay module 2624 preferably includes the switch 2650 and the capacitor 2652." '706, 28:24-25. But that sentence merely describes the claimed invention; it does not show the module to be a well-known structure to skilled artisans, and it does not even disclose a complete structure for down-converting ***and*** delaying (a single switch-capacitor pair is insufficient to both down-convert and delay). VDW ¶¶ 60-66.

Second, PV is wrong that dependent claims 3, 4, or 186 support PV's construction. Pl. Op. 8-9, 33-34. Those claims recite particular configurations of a switch and capacitor within a down-convert and delay module, but the fact that a dependent claim recites certain structure does not mean that an independent claim ***without*** that recited structure can avoid § 112 ¶ 6. *Nomos Corp. v. Brainlab USA, Inc*., 357 F.3d 1364, 1368–69 (Fed. Cir. 2004) ("[O]ur interpretation of the ***corresponding structure comes from the written description, not from dependent claim 3*** …."); *Mollhagen v. Witte*, 18 F. App'x 846, 849 (Fed. Cir. 2001) (nonprecedential) ("[T]he stringencies of a means-plus-function limitation cannot be avoided by merely adding a dependent claim that recites the corresponding

[6] PV asserts throughout its brief that a means-plus-function claim construction should not include citations to the specification text (column/line numbers) but rather only figure and/or structure numbers. That is wrong as a matter of law: "the specification must contain ***sufficient descriptive text*** by which a person of skill in the field of the invention would 'know and understand what structure corresponds to the means limitation.'" *Function Media LLC v. Google Inc.*, 708 F.3d 1310, 1317 (Fed. Cir. 2013). Intel's constructions properly provide the relevant "descriptive text" that identifies the specific structures that perform the claimed function. *Tomita Techs. USA, LLC v. Nintendo Co.*, 594 F. App'x 657, 663 (Fed. Cir. 2014) (nonprecedential) ("The correct corresponding structure should be: timing control unit 32 … and synthesis frame memory 50 described in Figure 3 and column 9 line 44 to column 10 line 29 and equivalents thereof.").

structure disclosed in the specification.").[7] Moreover, a skilled artisan would know that the single switch and capacitor disclosed in those dependent claims is insufficient to both down-convert and delay, as required by the claimed function.

B. "said input sample", "said sample" ('706 patent, claims 1, 6, 7, 34)

Proposed Constructions
Intel: "the sample of the image that has been down-converted" **PV:** Plain and ordinary meaning

The parties agree that the terms "said input sample" and "said sample" refer back to their respective antecedent bases in the claim—either "an input sample of a down-converted image of said input signal" or "a sample of a down-converted image of an input signal." Pl. Op. 9-10. Intel's proposed construction simply seeks to assist the jury by making this relationship clear—defining the "said input sample" or "said sample" as "the sample of the image that has been down-converted." PV argues that Intel is trying to "sever the relationship between the sample and the input signal." *Id.* at 10. To the contrary, Intel's construction applies the basic principle that a claim term must be construed consistently with its antecedent basis. *Process Control Corp. v. HydReclaim Corp.*, 190 F.3d 1350, 1356–57 (Fed. Cir. 1999) (noting importance of an antecedent basis in claim construction).

C. "delay module to delay instances of an output signal", "delay modules to further delay one or more of said delayed and down-converted input samples" ('706 patent, claims 1, 7, 34, 140)

Proposed Constructions
Intel: **Function**: delay instances of an output signal / further delay one or more of said delayed and down-converted input samples **Structure**: structure including "first delay module 2628," "second delay module 2630" shown in Fig 26, "delay module 3204" shown in Fig. 32 and described at 35:1-18; the sample and hold circuit 4501 and 4503 in Fig. 45 and described at 32:44-33:19; or an analog delay line having a

[7] PV cites *TEK Global v. Sealant Sys. Int'l, Inc.*, 920 F.3d 777, 786 (Fed. Cir. 2019), but the cited portion is dicta, as the case turned on the language of the independent claim. *Id.* ("We conclude that ***the language of claim 26, in and of itself***, does not indicate that § 112, ¶ 6 should apply.").

Proposed Constructions
combination of capacitors, inductors and/or resistors described at 35:19-27; or equivalents thereof that operates to delay samples/instances of a signal presented at its input by a known amount.
PV: Plain and ordinary meaning

The parties dispute whether the terms "delay module" and "delay modules" are means-plus-function terms (as Intel proposes) or whether those terms connote sufficiently specific structure to allow a "plain and ordinary meaning" construction (as PV argues).

Intel's Proposal. Both terms require means-plus-function construction because they claim in purely functional language—they recite "delay module(s)" to perform the function of "delay[ing] instances of an output signal" and "further delay[ing] one or more of said delayed and down-converted input samples." As explained above (*supra* II.A.), the word "module" is a well-known nonce word that operates as a substitute for "means"; the word "delay" simply describes a function of the module(s)—delay—without imparting any structure. *Williamson*, 792 F.3d at 1351 ("The prefix 'distributed learning control' does not impart structure into the term 'module.'"). Moreover, the term "delay module" does not have a well-understood specific structural meaning to skilled artisans VDW ¶ 70, and PV presents no evidence that it does. In fact, even the specification describes "delay module" in functional terms. '706, 32:26-29 ("3.4.2.2 Delay Modules. As indicated above, a delay module ***operates to delay*** samples/instances of a signal presented at its input by a known amount."). As a result, §112 ¶ 6 applies.

Intel's proposed functions for the terms track the claims directly. Intel's proposed structure comprises the structures disclosed in the specification for performing the claimed functions. The specification clearly links those functions to the "first delay module 2628" and "second delay module

2630" in Figure 26 and the "delay module 3204" in Figure 32.[8] '706, 32:30-43 ("[T]he first and second delay modules 2628 and 2630 ***operate to delay instances of the output signal VO***.");35:1-18 ("[W]hen using a switched capacitor such as [3204], the switch capacitor ***performs the function of…the delay module*** 1710, 1722."). The specification likewise clearly links the claimed "delay module(s)" to the sample and hold circuit 4501 and 4503 in Fig. 45 and an "analog delay line" having a combination of capacitors, inductors and/or resistors by teaching those structures as alternate implementations of "delay modules." *Id.*, 32:44-33:19 ("[T]he first delay module 2628 and the second delay module 2630 can each be implemented using either … 4501 or … 4503."); 35:19-27 ("The delay modules 1710, 1722 can also each be implemented using an analog delay line, such as the analog delay line 3404 in FIG. 34 …. The analog delay line 3404 operates to delay an input signal by a known amount.").

PV's Proposal. PV argues that a "delay module" has a "known structure that incorporates components/circuits, such as a ***capacitor***," citing Figures 17, 19, 23, 32, 34, and 34:60-35:31. But PV provides no evidence or otherwise explains what the allegedly known structure for a delay module is. In fact, there is no evidence that a "delay module" has a well-known specific structure. VDW ¶¶ 70-74. Moreover, none of the "delay modules" in the specification are simply a capacitor—the only specific structure PV mentions. Rather, each is a combination of components that "operates to delay an incoming signal by a predetermined amount." *Id.*, 34:64-67. For example, the patent states that delay modules can "be implemented using a switched capacitor topology 3204, such as that shown in FIG. 32," but that topology includes two switches 3208 and 3206 that operate according to a clock signal, two capacitors C1 and C2, and an amplifier. *Id.*, 35:1-6.

[8] PV argues that Intel's structure omits certain empty "black boxes" labeled "delay modules" in Figures 17, 19, and 23. Pl. Op. 11 n.7. But the specification teaches that those black box structures "can be implemented using a switched capacitor topology 3204," which is expressly ***included*** in Intel's structure. '706 patent, 35:1-6. PV's empty "black boxes" otherwise disclose no specific structure and would add nothing to the construction.

D. "harmonic", "harmonics" ('706 patent, claims 1, 6, 7, 28, 34; '508 patent, claim 1)

Intel's Proposed Construction	PV's Proposed Construction
Harmonic: "A sinusoidal component of a periodic wave that has a frequency that is an integer multiple of the fundamental frequency of the periodic wave"	**Harmonic:** "A sinusoidal component of a periodic wave that has a frequency that is an integer multiple of the fundamental frequency of the periodic waveform and including the fundamental frequency as the first harmonic"
Harmonics: "Sinusoidal components of a periodic wave each of which have a frequency that is an integer multiple of the fundamental frequency of the periodic wave"	**Harmonics:** "frequency or tone that, when compared to its fundamental or reference frequency or tone, is an integer multiple of it and including the fundamental frequency as the first harmonic"

The parties dispute whether the terms "harmonic"/"harmonics" should be construed consistent with the definition in the specifications (as Intel proposes) or whether the terms should be construed to require it to also include "the fundamental frequency as the first harmonic" (as PV proposes).

Intel's Proposal. Intel's proposed construction expressly tracks the patents' definition of "harmonic." In a section titled "Terminology," the '706 patent—*which the '508 patent incorporates by reference* ('508, 1:14-15, 1:25-27)—expressly defines "Harmonic: "A harmonic is a sinusoidal component of a periodic wave. It has a frequency that is an integer multiple of the fundamental frequency of the periodic wave." '706, 9:39-47. Consistent with Intel's proposed construction, the terms "harmonic" and "harmonics" should be construed according to this definition.[9] *Jack Guttman, Inc. v. Kopykake Enterprises, Inc.*, 302 F.3d 1352, 1360-61 (Fed. Cir. 2002) ("Where, as here, the patentee has clearly defined a claim term, that definition usually is dispositive; it is the single best guide to the meaning of a disputed term.").

[9] PV argues that Intel's proposal for the '508 patent "ignores the lexicography and, instead, improperly uses the lexicography from the '706 patent." Pl. Op. 14 n.12. But the '508 patent incorporates the '706 patent by reference, so the '706 lexicography ***is the '508 lexicography***. *Telemac Cellular Corp. v. Topp Telecom, Inc.*, 247 F.3d 1316, 1329 (Fed. Cir. 2001). Moreover, the parties do not contend that there is any substantive difference between the wording of the two definitions. Using one construction will be easier for the jury than using two distinct, but substantively identical, constructions.

PV's Proposal. PV proposes to construe "harmonic[s]" to also encompass "the fundamental frequency as the first harmonic." Pl. Op. 12-17. PV's attempt to expand the terms should be rejected.

First, while the patents recognize that the fundamental frequency is sometimes referred to as the "first harmonic," that is not how the patents use the term "harmonic[s]" in the context of the claimed invention. The parties agree that the patents define a harmonic to be a signal with a "frequency that is an ***integer multiple of the fundamental frequency***." '706, 9:39-41; '508, 9:53-55. The patents further state that a frequency at an ***integer multiple*** of the fundamental frequency is at a ***higher*** frequency than the fundamental frequency:

> As the harmonics have frequencies that are integer multiples of the repetition frequency of signal 1908, and since they have the same information content as signal 1908 (as just stated), ***the harmonics each represent an up-converted representation of signal 1908.***

'508, 17:60-64. That use of "harmonic" makes sense in the context of the claimed invention. PV's patents are directed to methods of up-conversion and down-conversion using harmonics. The '508 and '108 patents state, for instance, that "***[t]he up-conversion is accomplished***" by controlling a switch with an oscillating signal whose frequency "is selected as a ***sub-harmonic*** of the desired output frequency" and that "the desired ***harmonic*** is output." '508, Abstract;'108, Abstract ("A method and system is described wherein a signal ***with a lower frequency is up-converted to a higher frequency.*** … The up-conversion is accomplished by controlling a switch signal being selected as a ***sub-harmonic*** of the desired output frequency."). It is this conversion from the sub-harmonic to the harmonic that constitutes the up-conversion. If the sub-harmonic and harmonic could both be at the same fundamental frequency, as PV asserts, there would be no up-conversion at all—the system would output a signal with the same frequency as the input signal, which is directly contrary to the whole point of the claimed invention. '508, Abstract ("A method and system is described wherein a signal with a lower frequency is ***up-converted to a higher frequency***.").

Second, PV's proposed construction departs from the patents' definition of "harmonic." As explained above, the patents define "harmonic" as "an integer multiple of the fundamental frequency" of a periodic wave and do not include the language that PV proposes to add. '706, 9:39-41; '508, 9:53-55. PV argues that since the number 1 is an integer, the fundamental frequency must be a harmonic because the fundamental frequency is equal to itself multiplied by 1. Pl. Op. 16. But consistent with the object of the claimed inventions to up-convert a ***lower***-frequency signal to a ***higher***-frequency signal, both patents state—in the paragraphs that define "harmonic"—that the harmonics are "frequencies of 'n·f,' ***where 'n' is 2, 3, 4, etc.***":

> ***Harmonic:*** A harmonic is a sinusoidal component of a periodic wave. It has a frequency that is an integer multiple of the fundamental frequency of the periodic wave. In other words, ***if the periodic waveform has a fundamental frequency of 'f' (also called the first harmonic), then it has harmonics at frequencies of "n·f," where "n" is 2, 3, 4, etc.*** The harmonic corresponding to n=2 is referred to as the second harmonic, the harmonic corresponding to n=3 is referred to as the third harmonic, and so on.

'706, 9:39-47;'508, 9:53-61 (nearly identical language). PV's proposed language—"including the fundamental frequency as the first harmonic"—is therefore inconsistent with the patents' definition and should be rejected. *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996).

PV attempts to overcome the patents' definition by noting that Qualcomm agreed to PV's proposed construction in a separate litigation. Pl. Op. 16-17. But what a third party agreed to in a different litigation has no bearing on the proper construction of the term, particularly where the prior agreement is inconsistent with the express definition in the patents.

E. "pulse widths that are established to improve energy transfer" ('706 patent, claim 2)

Proposed Constructions
Intel: Indefinite **PV's:** Plain and ordinary meaning, or Pulse widths that use non-negligible apertures for energy transfer

Claim 2 of the '706 patent requires that the pulse widths in the control signal be "established

to improve" energy transfer in the down-conversion process. This claim term is indefinite because it fails to inform a person of skill in the art ***what*** constitutes an improvement in "energy transfer" or ***how*** to measure such an improvement. For example, is the improvement measured by the amount of energy transferred? By the rate at which the energy is transferred? No metric is defined. The claim also provides no baseline against which to measure the improvement. Must energy transfer be improved relative to some undefined prior-art system? *Interval Licensing LLC v. AOL, Inc.*, 766 F.3d 1364, 1373-74 (Fed. Cir. 2014) ("facially subjective claim language" indefinite where it lacked "objective boundary"). The claim's "established to" language creates further ambiguity. By requiring that pulse widths be "***established to*** improve energy transfer"—rather than just requiring "pulse widths that improve energy transfer"—the claim suggests that infringement turns on intentionality. Does a device infringe if pulse widths are established with the ***purpose*** to improve energy transfer but then do not actually do so? Does a device infringe if pulse widths improve energy transfer even if they were established without such a purpose? VDW ¶¶ 76-78.

PV argues that pulse widths "established to improve energy transfer" refer to pulse widths with non-negligible apertures because when such apertures are used, "more energy is transferred to a storage device." Pl. Op. 18. But PV's construction is inconsistent with independent claim 1, from which claim 2 depends. Claim 1 requires "under-sampling," which the '706 patent defines as the use of "***negligible*** apertures that tend towards zero time in duration." '706, 1:6-12 (incorporating USP 6,061,551) (Ex. 4); Ex. 4, 63:5-7. PV's construction for claim 2 thus requires the impossible—that the apertures be both non-negligible and negligible at the same time—and the claim is therefore indefinite.

F. "means for under-sampling an input signal to produce an input sample of a down-converted image of said input signal" ('706 patent, claim 6)

Intel's Proposed Construction	PV's Proposed Construction
Function: under-sampling an input signal to produce an input sample of a down-converted image of said input	**Function:** under-sampling an input signal to produce an input sample of

Intel's Proposed Construction	PV's Proposed Construction
signal and under-sampling the input signal according to a control signal **Structure:** the switch 2650 and the capacitor 2652 in Fig. 26 and described at 26:1-27:21 and 28:20-28; the switch 5308 and capacitor 5310 in Fig. 53A and described at 28:46-47; the switch 5308 and capacitor 5310 in Fig. 53A-1 and described at 28:52-56 and equivalents thereof.	a down-converted image of the input signal and under-sampling the input signal according to a control signal **Structure:** switch 2650 in Fig. 26; switch 5308 in Figs. 53A/53A-1; and equivalents thereof

The parties dispute whether the structure performing this function consists of both a switch and a capacitor (as Intel proposes) or whether it covers a switch alone (as PV proposes).[10]

Intel's Proposal. Claim 6 requires a "frequency translator" comprising (a) a means for under-sampling an input signal to produce an input sample of a down-converted image of the input signal (the term at issue here); and (b) a means for delaying the resulting input sample (the next term). Both parties agree that the specification describes two embodiments for performing the first function (i.e., under-sampling to down-convert): (1) down-convert and delay module 2624 in Figure 26, and (2) aliasing module 5300 in Figures 53A and 53A-1. Pl. Op. 20-22. In both embodiments, the structure for under-sampling to down-covert is described and shown as a switch ***and a capacitor***.

In Figure 26 (shown below), the down-convert and delay module 2624 includes (a) a first switch 2650 and capacitor 2652 (highlighted in pink) that perform the function required by this claim term (under-sampling to down-convert), followed by (b) a second switch 2654 and capacitor 2656 that perform the function required by the next term (delaying the resulting input sample).

[10] PV criticizes Intel for excluding Figures 53A and 53A-1 from its construction. But prior to filing its brief, even PV never took the position that it believed Figures 53A and 53A-1 should be included. (PV modified its proposed construction for the first time in its opening brief without prior disclosure to Intel.) Intel does not oppose including a reference to Figures 53A and 53A-1.

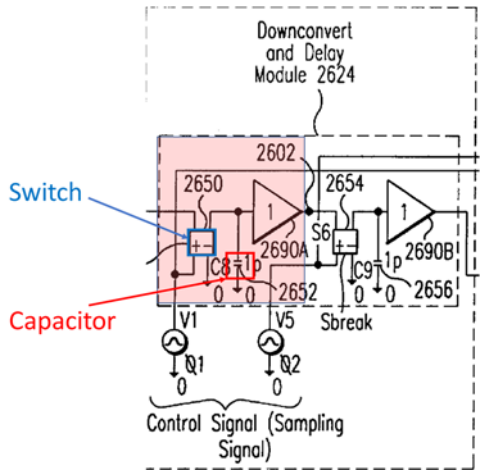


Fig. 26 (excerpted). The specification describes the first switch and capacitor ***together*** as performing the under-sampling to down-convert function: '706, 28:24-28 ("[T]he switch 2650 ***and the capacitor 2652 operate to down-convert*** the input signal VI."); 26:5-8 ("***[T]he combination of the switch 2650 and the capacitor 2652*** in the down-convert and delay module ***2624 operates to translate the frequency*** of the input signal VI to a desired lower frequency."). Similarly, the patent describes aliasing module 5300 in Figure 53 as "a universal frequency ***down-conversion module***" (*id.*, 28:43-44) and states that "aliasing module 5300"—switch 5308 ***and*** capacitor 5310—performs the under-sampling to down-convert. *Id.,* 28:61-67 ("In one implementation, aliasing module 5300 down-converts the input signal 5304 to an intermediate frequency (IF) signal. In another implementation, the aliasing module 5300 down-converts the input signal 5304 to a demodulated baseband signal. In yet another implementation … the aliasing module 5300 down-converts it to a non-FM signal.").

PV argues that only the switch performs "under-sampling" and that the capacitor merely receives energy from the switch. Pl. Op. 21-22. But that argument is inconsistent with PV's own description of under-sampling. In the '551 patent, which the '706 patent incorporates by reference, PV states that "the switch module 2702 and the holding module 2706 [i.e., capacitor] ***cooperate*** to under-sample the EM signal 1304 and down-convert it to an intermediate signal." '551, 55:6-8, 63:41-

44("***[U]nder-sampling system 7802*** includes ***a switching module 7806 and a holding module*** shown as a holding capacitance 7808."), 54:51-53.

PV's argument also incorrectly tries to divorce under-sampling from down-conversion. The claimed function is not merely "under-sampling" but under-sampling "to produce an input sample of a ***down-converted image*** of said input signal." Moreover, under-sampling to down-convert a signal could not occur absent the capacitor. '706, 29:18-22 ("When the switch 5308 is closed … charge is transferred from the input signal to the capacitor 5310. ***The charge stored during successive pulses forms down-converted output signal 5312***."); VDW ¶¶ 80-83.

PV is also wrong that Intel's construction improperly "restrict[s] the equivalents analysis" by not including three passages from the patent. Pl. Op. 22. Intel has no objection to adding the passage at column 39:25-28, which clearly describes the down-conversion being "performed essentially by a switch 2650 ***and*** a capacitor 2652." '706, 39:25-28. The other two passages (24:40-25:67 and 29:4-8) focus primarily on the control signals and convey nothing about the structure for performing the relevant function beyond what Intel's construction already contains.

PV's Proposal. PV's proposed construction should be rejected because it excludes the capacitors in Figures 26 and 53/53A-1. PV's argument is based on a single sentence from the patent, which PV misreads. The sentence states that "FIG. 53A illustrates an aliasing module 5300 (also called in this context a universal frequency down-conversion module) for down-conversion using a universal frequency translation (UFT) module 5302 which down-converts an EM input signal 5304." Pl. Op. 22 (citing '706, 28:42-46). PV interprets "which down-converts an EM input signal 5304" as modifying UFT module 5302—which consists of switch 5308. But the surrounding context makes clear that although aliasing module 5300 "***us[es]***" the UFT module 5302 (switch 5308) to down-convert, it is the aliasing module—which includes ***both*** switch 5308 and capacitor 5310—that down-converts. '706

patent, 28:61-67 ("***[A]liasing module 5300 down-converts the input signal*** 5304.").[11]

Finally, PV has conceded that the capacitor is a necessary part of the down-conversion process. In PV's opening brief in the -108 case, PV described the "capacitor" as an "***essential***" component in generating the down-converted signal:

> The waveform [down-converted signal 8310] is made up of energy [] from the EM signal and discharged energy [] from the 'storage' capacitor. Indeed, the ***discharged energy [] from the 'storage' capacitor is essential. Without the discharged energy, the waveform of Figure 83E would be incomplete*** ….

No. 20-cv-108, Dkt. 51 at 8.

G. "first delaying means for delaying said input sample" ('706 patent, claim 6)

Intel's Proposed Construction	PV's Proposed Construction
Function: delaying said input sample **Structure**: the switch 2654 and capacitor 2656 shown in Fig. 26 and described at 25:57-27:21 and 28:20-28; and equivalents thereof.	**Function:** delaying the input sample of a down-converted image of said input signal **Structure:** capacitor 2656 in Fig. 26 of capacitor 5310 in Figs. 53A/53A-1; and equivalents thereof

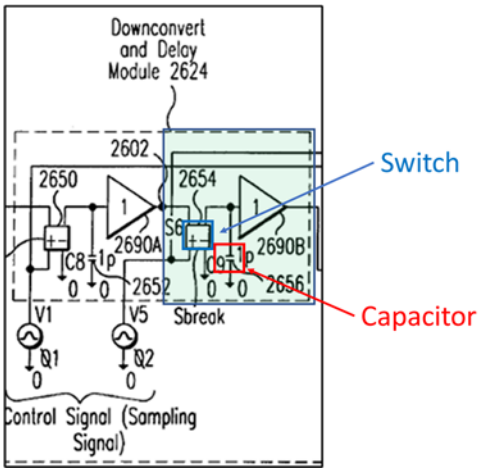
The parties agree that this term should be construed as means-plus-function and substantively agree about the function.[12] The parties dispute whether the proper structure consists of both a switch and a capacitor (as Intel proposes) or whether it includes only a capacitor (as PV proposes).

Intel's Proposal. The claims describe the "first delaying means" as part of the frequency

[11] PV suggests the capacitor in Figure 53 is not involved in down-conversion because the figure is allegedly an "energy transfer" embodiment that uses non-negligible apertures. Pl. Op. 21. But Figure 53 is expressly described in the patent as using negligible apertures. '706, 32:4-5 ("In an embodiment, the pulses of the control signal 5306 have negligible apertures that tend towards zero."), 29:34-38. Moreover, the incorporated '551 patent clearly describes how a switch and capacitor (i.e., storage module) ***together*** perform down-conversion in an energy transfer embodiment: "***the switch module 7404 and the storage module 7406*** transfer energy from the EM signal 1304 ***to down-convert it***." '706, 101:55-57.

[12] PV states that the parties disagree on this function (Pl. Op. 23), but PV never disclosed its proposed function to Intel before filing its brief. Intel's proposed function adopts the language of the claim verbatim: "the first delaying means ***for delaying said input sample***." PV replaces "said input sample" with its antecedent: "an input sample of a down-converted image of said input signal." Intel does not believe there is substantive difference between the two functions.

translator, which as explained above, corresponds to the "down-convert and delay module" described in the patent. As discussed in the previous section, the first part of the "down convert and delay module" (switch 2650 and capacitor 2652) performs the first function of under-sampling to produce a down-converted input sample. The second part of the module (shown below in green), performs the second function: delaying the down-converted input sample.



As shown, the "first delaying means" portion consists of both a switch (2654) and a capacitor (2656). The switch is critical to the operation of the delay function. When open, switch 2654 prevents the down-converted image (i.e., the input sample) from being transferred to the capacitor 2656, thereby delaying the sample. When closed, switch 2654 allows the down-converted image to transfer to the capacitor. '706, 26:25-30 ("At the rising edge of ϕ2 at time t-1, a switch 2654 in the down-convert and delay module 2624 closes, allowing a capacitor 2656 to charge to the level of the capacitor 2652."), 27:1-6. If the switch were omitted—as in PV's construction—there would be no delay. The input sample would immediately transfer from the first switch (2650) directly to the capacitor in the "first delaying means" (2656), just as it does when the switch is closed. It is therefore switch 2654 ***and*** capacitor 2656 together that perform the function of "delaying of said input sample." VDW ¶¶ 84-86.

PV argues that Intel's construction omits a reference to the passage at column 24:40-25:56 and

thereby "restrict[s] the equivalents analysis." Pl. Op. 25. But that passage does not identify any structure for a "first delaying means" beyond what is already disclosed in Intel's construction.

PV's Proposal. PV's proposed construction *excludes* necessary structure and *includes* figures that are not relevant. ***First,*** PV's proposal improperly excludes a necessary component—switch 2654. As described above, the switch is crucial to the delay function; without the switch, there is no delay. Moreover, even PV concedes that the switch plays a role in delaying the sample because, as PV notes, the capacitor will not discharge ***until*** the switch opens. Pl. Op. 24-25 ("[T]he input sample (red arrow) is sent to capacitor 5310 where it is stored (delayed) until, as shown in Figure 53A (above right), the switch 5308 turns OFF (opens) and the switch [sic] discharges energy (orange arrow)."). In short, the delay is caused by the ***coordination*** of the two components—the switch closing and opening and the capacitor charging and discharging the stored energy. By excluding the switch, PV's construction eliminates structure necessary to perform the claimed function. ***Second***, PV's proposed structure includes capacitor 5310 in Figures 53A and 53A-1. But Figures 53A and 53A-1 embody a structure for ***producing a down-converted input sample*** discussed in Section II.F. above, not the structure required for the function of this claim limitation—i.e., ***delaying*** the down-converted input sample. The patent describes Figures 53A and 53A-1 as "illustrat[ing] an aliasing module 5300 (also called in this context a universal frequency down-conversion module) ***for down-conversion***." '706, 28:42-44.

H. "second delaying means for delaying instances of an output signal" ('706 patent, claim 6)

Intel's Proposed Construction	PV's Proposed Construction
Function: delaying instances of an output signal **Structure**: structure including "first delay module 2628," "second delay module 2630" shown in Fig 26 and described at 32:27-55, "delay module 3204" shown in Fig. 32 and described at 35:1-18; the sample and hold circuits 4501 and 4503 in Fig. 45 and described	**Function:** delaying instances of an output signal **Structure**: delay modules 1722A, 1722B, 1722C, etc. in FIG. 17; delay modules 1912, 1914 in Fig. 19; delay modules 2316, 2318 in Fig. 23; first delay module 2628, second delay module 2630 in Fig. 26; delay module 3204 shown in Fig. 32; sample and hold circuits 4501, 4503 shown in

Intel's Proposed Construction	PV's Proposed Construction
at 32:44-64; or an analog delay line having a combination of capacitors, inductors and/or resistors described at 35:19-27; and equivalents thereof.[13]	Fig. 45; analog delay line 3404 shown in Fig. 34 having a combination of capacitors, inductors, and/or resistors; and equivalents thereof

The parties dispute whether the structure for this claim term can simply be a generic "black box" that encompasses any circuitry that performs the claimed function (as PV proposes) or whether it requires the specific structures identified in the patent (as Intel proposes).

Intel's Proposal. Claim 6 recites "an apparatus for filtering and down-converting, comprising … a filter, comprising: … (b) ***second delaying means for delaying instances of an output signal***." The patent provides a list of structures that perform the claimed function of "delaying instances of an output signal." For example, in a section titled "Delay Modules," the '706 patent states that "in the embodiment of the UFD module 2622 shown in FIG. 26 [below], the ***first and second delay modules 2628*** [red] ***and 2630*** [blue] ***operate to delay instances of the output signal*** VO." *Id.*, 32:30-33.

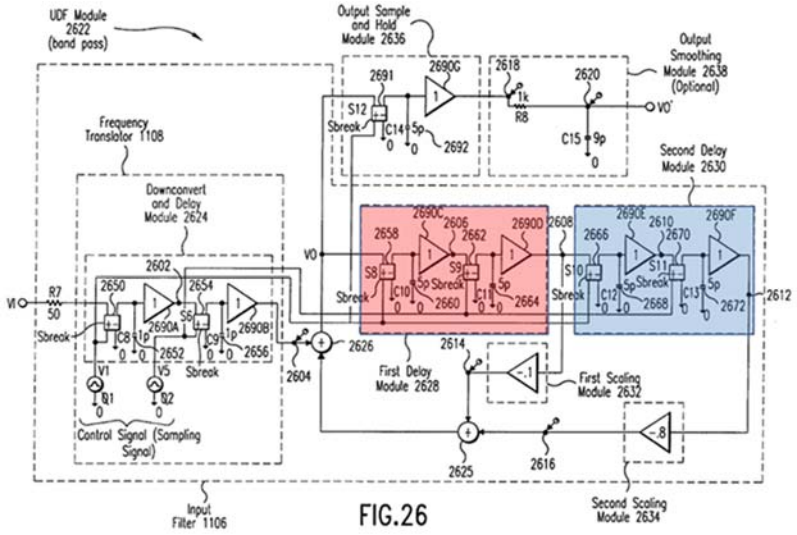
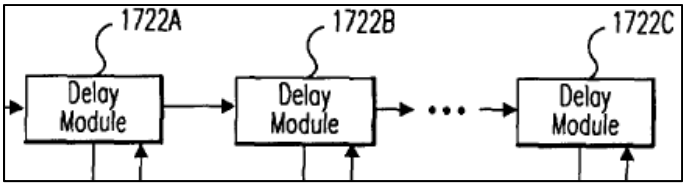


FIG.26

[13] Intel has revised its construction to include the patent's description of the first and second delay modules (2628 and 2630), and to clarify the description of the analog delay line based on that structure's description in the specification. In addition, to narrow the claim construction issues, Intel has removed the following language from its construction: "that operate to delay samples/instances of a signal presented at its input by a known amount."

Both delay modules are shown as having a specific circuit structure, and the patent states that delay modules can also be implemented with other specific circuit structures identified in the patent: sample-and-hold circuits 4501 and 4503 (*id.*, 32:44-61); delay module 3204 (*id.*, 25:2-17), or an analog delay line "constructed using a combination of ***capacitors, inductors, and/or resistors***" (*id.*, 35:19-24). The patent does not identify any other specific structures that perform the claimed function, and Intel's proposed construction accurately includes the three structures that are disclosed.[14]

PV's Proposal. PV's proposed construction should be rejected. ***First***, PV's construction includes empty "black boxes" that, as shown below, have no specific circuitry or structure and provide no indication of what is inside the box, how the box works, or how the box is supposed to perform the claimed function.



These "black box" figures cannot provide the necessary structure in a means-plus-function analysis. *Mettler–Toledo, Inc. v. B–Tek Scales, LLC,* 671 F.3d 1291, 1295–96 (Fed. Cir. 2012) (affirming construction limiting a means-plus-function limitation to specific disclosed analog-to-digital converter, despite presence of generic "analog-to-digital converter" figure in patent.); *Bennett Marine, Inc. v. Lenco Marine, Inc.*, 549 F. App'x 947, 954 (Fed. Cir. 2013) (nonprecedential) (limiting structure for means-plus-function term to "specific circuit shown in figure 2" rather than to "the generic circuit shown in figure 1, i.e., any circuit fulfilling the required function"). In addition, the patent describes these modules only in terms of what function(s) they perform. VDW ¶ 92. ***Second***, PV's proposed

[14] PV argues that Intel allegedly "omit[s] several columns of discussion regarding the structure of the circuits," including for example col. 32:65-34:59. Pl. Op. 30. But those columns do not describe any structure for performing the claimed function; they discuss Figure 46, which is simply a generic flowchart. '706, 33:20-22; Fig. 46.

construction fails to include the patent's descriptions of the claimed structures. As explained, *supra* II.A, a means-plus-function term must have a sufficiently definite structure. This requires tying the figures in the patent with the patent's descriptions of those figures. *Noah Sys.*, 675 F.3d at 1311.

I. "integral filter/frequency translator to filter and down-convert an input signal" ('706 patent, claim 28)

Proposed Constructions
Intel: **Function**: to filter and down-convert an input signal **Structure**: the Unified Downconvert and Filter (UDF) Module 2622 that includes: (1) the frequency translator 1108 having the down convert and delay module 2624; (2) a first delay module, including the delay module 2628 shown in Fig. 26, the delay module 3204 shown in Fig. 32 and described at 35:1-18, the sample and hold circuit 4501 or 4503 shown in Fig. 45 and described at 32:44-64, or the analog delay line having a combination of capacitors, inductors and/or resistors described at 35:19-27 that operates to delay samples/instances of a signal presented at its input by a known amount; (3) a second delay module including the delay module 2630 shown in Fig. 26, the delay module 3204 shown in Fig. 32 and described at 35:1-18, the sample and hold circuit 4501 or 4503 shown in Fig. 45 and described at 32:44-64, or the analog delay line having a combination of capacitors, inductors and/or resistors described at 35:19-27 that operates to delay samples/instances of a signal presented at its input by a known amount; (4) a first scaling module, including the first scaling module 2632 shown in Fig. 26, the resistor attenuator 3602 shown in Fig. 36 and described at 35:44-55, or the amplifier/attenuator 3704 implemented using operational amplifiers, transistors, or FETs shown in Fig. 37 and described at 35:60-67; (5) a second scaling module, including the second scaling module 2634 shown in Fig. 26, the resistor attenuator 3602 shown in Fig. 36 and described at 35:44-55, or the amplifier/attenuator 3704 implemented using the operational amplifiers, transistors, or FETs shown in Fig. 37 and described at 35:60-67; (6) a first adder including, the adder 2625 in Fig. 26, adder 1720 in Fig. 17, the adder 2522 in Fig. 25, the summer 3902 in Fig. 39, or the summer 4102 in Fig. 41; and (7) a second adder, including the adder 2626 in Fig. 26, adder 1720 in Fig. 17, the adder 2522 in Fig. 25, the summer 3902 in Fig. 39, and the summer 4102 in Fig. 41; and equivalents thereof. **PV:** "a circuit in which the input filtering operation is integrated with the frequency translation operation"

The parties dispute whether the term should be construed as means-plus-function (as Intel proposes) or should be construed as "a circuit having a unified input filter and frequency translator," which effectively ignores the recited function (as PV proposes).

Intel's Proposal. PV claims to have invented an integrated filter and frequency translator in the '706 patent. '706, Title ("***Integrated Frequency Translation and*** Selectivity [i.e., filtering]"), Abstract ("The filtering and the down-conversion operations are performed in an integrated, unified manner."), 10:26-34 ("***According to the present invention***, frequency selectivity [i.e., filtering] ***and frequency translation*** [i.e., down-conversion] are performed as a ***single unified (i.e., integrated) operation***."), 12:14-15 ("***The present invention*** is directed to methods and apparatuses for ***unified down-converting and filtering (UDF)***."). But the disputed limitation of Claim 28 says nothing about what an "integral filter/frequency translator" is; it simply recites what the alleged invention does in functional language: "[A]n integral filter/frequency translator ***to filter and down-convert an input signal***." '706, Cl. 28.

The term "integral filter/frequency translator" does not connote any specific structure, let alone two separate structures (i.e., a "filter and frequency translator"), as PV argues. The term was coined by PV, and as PV essentially admits in its brief, the term refers to a device defined solely in functional terms: a device in which the "operations—filtering/frequency selection and frequency translation—are performed 'concurrently.'" Pl. Op. 32. As explained above, even the sub-term "frequency translator" does not have a sufficiently definite meaning as the name of a structure. Moreover, the entire point of the '706 patent is to describe a purportedly new structure that PV claims was not known in the prior art for performing the claimed function: an "***integral*** filter/frequency translator." Thus, the term "integral filter/frequency translator" does not have a well-understood meaning. VDW ¶¶ 94, 97. PV cannot avoid means-plus-function by coining a purported structural term, and then using that term to try to cover any device that performs the claimed function—that is directly contrary to the purpose of § 112 ¶ 6. *Blackboard, Inc. v. Desire2Learn Inc.*, 574 F.3d 1371, 1385 (Fed. Cir. 2009) ("To allow that form of claiming under section 112, paragraph 6, would allow the patentee to claim all possible

means of achieving a function.").

Intel's proposed construction for the function of this term tracks claim 28 verbatim: "to filter and down-convert an input signal." Intel's proposed construction recites the structure disclosed in the specification as necessary to perform that function—the ***unified down-converting and filtering*** (***UDF***) module 2622 in Fig 26 (highlighted below):

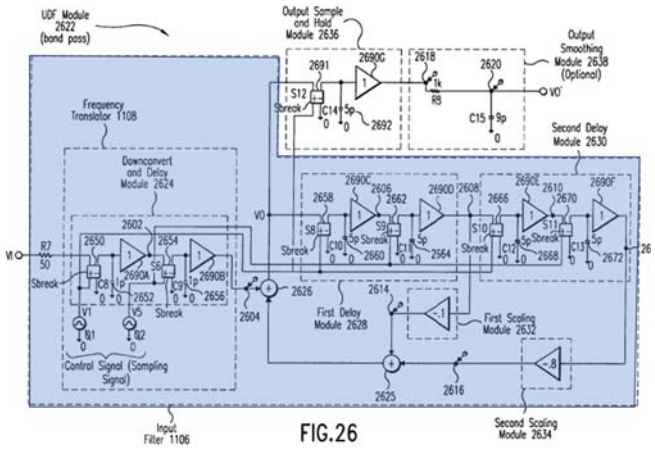


FIG.26

'706, Fig. 26, 24:24-47 ("FIG. 26 illustrates an example implementation of the unified down-converting and filtering (UDF) module 2622. ***The UDF module 2622 performs the frequency translation operation 1204 and*** the frequency selectivity operation 1202 [i.e., ***filtering***] ***in an integrated, unified manner*** as described above, and as further described below."). Intel's proposed structure consists of the components in the UDF module 2622 in Figure 26[15] and equivalent structures disclosed in alternate embodiments.

The UDF module in Figure 26 is the only structure disclosed in the '706 patent to achieve the functions of "filter[ing] and down-convert[ing] an input signal." *Williamson*, 792 F.3d at 1352 ("Even if the specification discloses corresponding structure, the disclosure must be of 'adequate'

[15] The frequency translator 1108, the (first) "delay module 2628," the (second) "delay module 2630," the "first scaling module 2632," the "second scaling module 2634," the (first) "adder 2625," and the (second) "adder 2626."

corresponding structure to achieve the claimed function."). No other figure in the specification shows the actual structures—i.e., the switches, capacitors, scaling modules, and adders—that down-convert and delay an input sample. '706, 24:40-37:9. Thus, this term should be construed as limited to the structure disclosed in Figure 26, the corresponding specification descriptions, and the equivalents of those expressly defined structures.

PV's Proposal. PV's proposed construction is flawed for two reasons. ***First***, the term "integral filter/frequency translator" must be means-plus-function because claim 28 is written in functional terms without sufficient structure to perform the claimed function. ***Second***, PV coined a purported structural term ("integral filter/frequency translator") and is now trying to use that term to cover any device that performs the claimed function; that is exactly what § 112 ¶ 6 prohibits. *Blackboard*, 574 F.3d at 1384.

J. "modulated signal" ('706 patent, claim 127)

Proposed Constructions
Intel: "a signal with physical characteristics varied to represent the transmitted information"
PV: "an electromagnetic signal at a transmission frequency having at least one characteristic that has been modulated by a baseband signal"

In a section entitled "Terminology," the '706 patent defines the term "modulation" as "[t]he process of ***varying*** one or more ***physical characteristics*** of a signal ***to represent the information to be transmitted***." '706, 9:58-60. Intel's proposed construction for "modulated signal" closely tracks this definition and should therefore be noncontroversial: "a signal with ***physical characteristics varied to represent the transmitted information***." PV's proposed construction for "modulated signal" is based on the Court's construction for a ***different*** term ("modulated carrier signal") that, because it includes the word "carrier," is necessarily narrower than the term at issue here.

K. "filter tuning means for tuning one or more filter parameters" ('706 patent, claim 134)

Intel's Proposed Construction	PV's Proposed Construction
Function: tuning one or more filter parameters **Structure**: scaling modules including the resistor attenuator 3602 (shown in Fig. 36 and described at 35:44-55) or the amplifier/attenuator 3704 implemented using operational amplifiers, transistors, or FETS (shown in Fig. 37 and described at 35:60-67), each of the resistor attenuator 3602 and the amplifier/attenuator 3704 having tunable resistors, capacitors, or inductors (as described at 42:33-36); and equivalents thereof; **OR** the control signal generator 4202 (shown in Fig. 42 and described at 36:44-62 and 42:27-32) implemented with a tunable oscillator 4204 and an aperture optimizing module 4210 using tunable components (such as tunable resistors, capacitors, inductors, etc.) (described at 36:63-37:5 and 42:27-32) and equivalents thereof.	**Function:** tuning one or more filter parameters **Structure:** scaling modules 1716A, 1716B, 1716C, 1724A, 1724B, 1724C, etc. in Fig. 17; input scaling module 1909 in Fig. 19; scaling modules 1916, 1918 in Fig. 19; scaling modules 2312, 2320, 2322 in Fig. 23; scaling modules 2510, 2518, 2520 in Fig. 25; scaling module 2632, 2634 in Fig. 26; scaling module 3502 in Fig. 35; scaling module 3702 in Fig. 37; control signal generator 1790 in Fig. 17; control signal generator 4202 in Fig. 42; and equivalents

The parties agree that the corresponding structure for this term includes scaling modules and the control signal generator 4202 that are linked in the '706 patent to the claimed "tuning" function. PV, however, incorrectly asks the Court to add other structures ***not*** linked to the tuning function.

Intel's Proposal. "Structure disclosed in the specification qualifies as 'corresponding structure' if the intrinsic evidence ***clearly links*** or associates that structure ***to the function recited in the claims***." *Williamson*, 792 F.3d at 1352. The claimed function—"***tuning*** one or more filter parameters"—necessarily requires ***tuning***, and Intel's construction therefore includes the structures that the specification discloses as ***tunable***: (1) scaling modules that include ***tunable*** resistors, capacitors, or inductors (described at 42:33-36), and (2) a control signal generator implemented with (a) a ***tunable*** oscillator, and (b) an aperture optimizing module using ***tunable*** components (such as ***tunable*** resistors, capacitors, inductors, etc.) (described at 36:44-62 and 42:27-32). The patent clearly links these components—and only these components—to the function of "***tuning*** one or more filter parameters." '706, 42:27-36.

PV's Proposal. PV's proposal (and its corresponding criticisms of Intel's construction) are

incorrect. ***First,*** PV criticizes Intel's construction (Disputes 1 and 2) for allegedly excluding various scaling modules identified in Figures 17, 19, 23, 26, and 35. Pl. Op. 37-38. But Intel's proposed construction does not exclude any specific scaling module: it refers to "scaling modules" generally and thus covers any scaling module provided that it contains the ***tunable*** components that the specification "clearly links" to the claimed function. *Williamson*, 792 F.3d at 1352. ***Second,*** PV is wrong to criticize Intel's construction (Disputes 4 and 5) for requiring that certain devices in the scaling modules and control signal generator be tunable and/or use tunable components. Pl. Op. 40-43. PV notes (correctly) that the specification includes embodiments that are not tunable. But the claim term at issue requires a "filter ***tuning*** means for ***tuning*** one or more filter parameters." Only the ***tunable*** embodiments are clearly linked to the claimed tuning function and can constitute corresponding structure.[16] *Williamson*, 792 F.3d at 1352.

Third, PV mistakenly criticizes Intel's construction (Dispute 3) for requiring that the amplifier/attenuator 3704 be "implemented using operational amplifiers, transistors, or FETS." Pl. Op. 39-40. PV cites specification language stating that amplifiers are "not limited to" such components ('706, 35:63-67), but this is a means-plus-function claim, which is limited in scope to the specific

[16] PV argues that "aperture optimizing module 4210" should not be included because it is labeled "optional" in Figure 42. Pl. Op. 42-43. But the patent describes the aperture optimizing module 4210 as used in tuning embodiments to "adjust the aperture (width) of the pulses" '706, 36:63-37:1, so for the tuning function at issue here, the module is corresponding structure. Nor is Intel "attempting to read a limitation from dependent claim 138 into dependent claim 134." Pl. Op. 40. Claim 134 requires a "filter tuning means," and claim 138, which depends from claim 134, further recites that the "filter tuning means" comprises "means for adjusting at least one scale factor." For claim 134, Intel properly proposed structures that are clearly disclosed in the specification as "tunable." PV, on the other hand, takes the paradoxical position that "'tunable' components are ***not*** part of the "filter ***tuning*** means for ***tuning***" in claim 134, and are instead only part of the "means for ***adjusting***" in claim 138 (Pl. Op. 41).

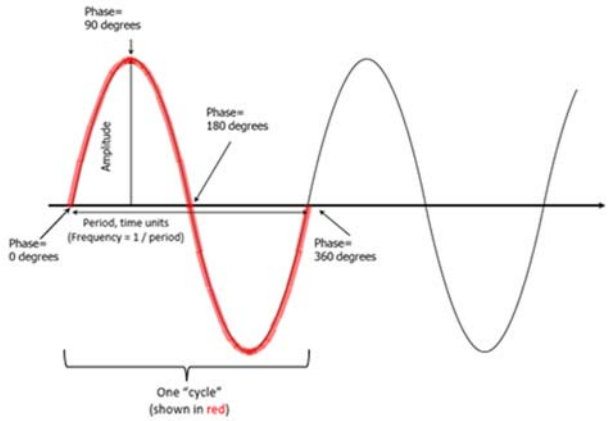
disclosed structure and its equivalents.[17]

III. THE ASSERTED TRANSMITTER PATENTS

U.S. Patent No. 8,190,108 (the '108 patent) and U.S. Patent No. 7,050,508 (the '508 patent) are directed to apparatuses and methods used in "up-conversion"—a process by which a low-frequency signal is shifted to a higher frequency so that the signal can be transmitted wirelessly.

A. Frequency Up-Conversion

Wireless devices, such as cellular phones, communicate by transmitting and receiving electromagnetic (EM signals). VDW ¶ 101. An exemplary EM signal (or "EM wave") is shown below:



Id. Wireless devices use EM signals to carry information such as voice messages, images, or other data over the air from one electronic device to another. *Id.* All EM signals have basic properties, such as phase, amplitude, and frequency. As shown in the figure above, an EM signal will oscillate between peaks and valleys. One complete oscillation of the signal in this manner is referred to as a "cycle" of the signal. The signal's "phase" refers to the current location of the signal within a cycle as it oscillates. The signal's "amplitude" refers to how much the signal deviates between its equilibrium value to its

[17] In an effort to narrow the issues for the Court and in view of the similarity in the parties' proposed constructions, Intel will accept PV's proposal for the term "energy transfer signal comprising a train of pulses." It is established patent law that the definition of the term "comprising" is "including"; thus, there is no need for the Court to address this issue.

peak or valley. The signal's "frequency" refers to the number of cycles the signal completes within a unit of time. The greater the number of oscillations per unit of time, the higher the frequency. *Id.* ¶ 102.

Before an EM signal is transmitted, it exists in the wireless device in the form of a "baseband signal" or "information signal." *Id.* ¶ 101; '108, 7:44-50. Baseband signals carry the information—such as voice information—to be transmitted. A baseband signal is typically created with a process called "modulation" in which characteristics of the EM signal are modified so that the signal represents the information to be transmitted. VDW ¶ 103-105; '108, 8:61-66.

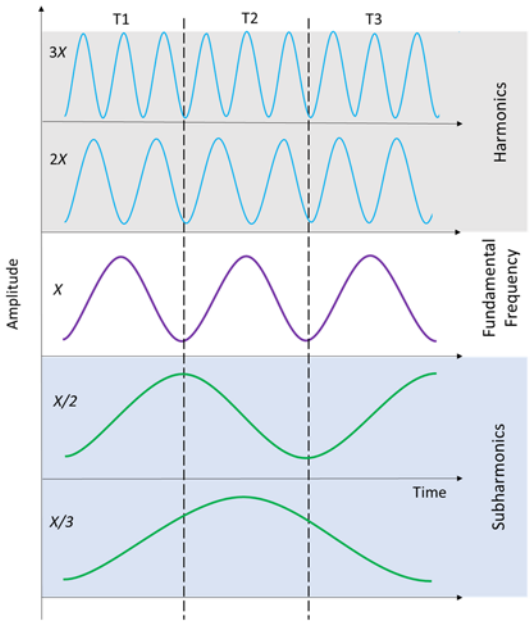
Baseband signals have a low frequency. Low-frequency signals cannot be easily transmitted and do not travel well over long distances. High-frequency signals, such as radio frequency or "RF" signals, on the other hand, can be more easily transmitted and thus are effective for wireless communications. As a result, to transmit data wirelessly, baseband signals are typically shifted to a higher frequency RF signal and then transmitted. The process of shifting a lower-frequency signal to a higher-frequency is called "up-conversion." VDW ¶ 106; '108, 9:43-46.

B. Basic Techniques for Up-conversion

As the patents acknowledge, up-conversion was well-known in the prior art. '108, 14:1-6; '508, 15:32-37. There were many known ways of up-conversion before the claimed inventions. '108, 1:44-51, 10:50-11:2, 13:48-14:6; '508, 1:55-63, 12:12-32, 15:12-37; VDW ¶ 116-17. One known technique involves the use of a high-frequency oscillator and a mixer. The oscillator creates a signal at the desired transmission frequency. The mixer then "mixes" this high-frequency signal with the signal carrying the information resulting in the up-conversion of the lower-frequency signal carrying the information to the higher frequency of the oscillator signal. VDW ¶ 118.

Another known technique—which is the subject of the transmitter patents—involves the creation of "harmonically rich signals." A "harmonically rich signal" includes multiple components

that are each "harmonics" of the initial signal frequency. "Harmonics" are signals that are representations of the original signal but with frequencies that are integer multiples of the initial frequency. For example, if the initial signal has frequency X, called the "fundamental frequency," then its harmonics can have frequencies of 2X, 3X, 4X etc. as shown in the first two rows of the graph below. Conversely, "sub-harmonics" are signals with frequencies that are integer sub-multiples of the initial frequency. For example, if the initial signal has a frequency X, its sub-harmonics can have frequencies of (1/2)X, (1/3)X, and (1/4)X etc. as shown in the last two rows of the graph below.



Id. ¶ 108. Generating a harmonically rich signal is one way to up-convert a signal because the harmonically rich signal includes harmonics having frequencies of 2X, 3X, 4X, etc. Any of those harmonic signals can be extracted from the harmonically rich signal to obtain an up-converted version of the initial signal. *Id.* ¶ 110.

C. '508 Patent Overview[18]

[18] Because the '508 patent builds on the technology described in the '108 patent, Intel suggests reviewing the '108 background and disputed terms beginning on p. 49 below before returning to the '508 patent section. Intel proposed ordering the brief in this way, but PV refused.

The '508 patent is a continuation-in-part of the '108 patent's parent, the '940 patent. Like the '108 patent (described below), the '508 patent purports to have invented a more efficient method for up-converting a signal for transmission. As described in detail below, the system in the '108 patent up-converts a signal by generating a harmonically rich signal that includes multiple harmonics—each of which is a representation of the original signal but at a higher frequency—and then selects one of the harmonics to use as the desired (and up-converted) output signal. The '108 patent explains that, to accomplish up-conversion, the harmonically rich signal is generated by a switch controlled by a "control signal." The patents explain that the control signal must have a frequency that is ***lower than*** and a ***sub-harmonic*** of the desired output frequency in order to create the desired harmonically rich signal. '508, 2:21-52.

The '508 patent repeats much of the up-conversion description in the '108 patent. The '508 patent, however, introduces an additional component called a "multiple aperture generation module." '508, Fig. 78. The multiple aperture generation module is inserted between the "pulse shaper" and the switch in Fig. 54A. The patent asserts that the aperture generation module "optimiz[es]" the amplitude of the harmonic waveform. '508, 49:43-45. Specifically, the aperture generation module ***increases*** the amplitude of the ***desired*** harmonic, and ***decreases*** the amplitude of the ***undesired*** harmonics, which purportedly allows for improved filtering for the desired harmonic. *Id.*, 50:38-40 ("As can be seen, the desired harmonic amplitude is increased and the undesired harmonics decreased as a function of the number of pulses per cycle."), 44:13-17.

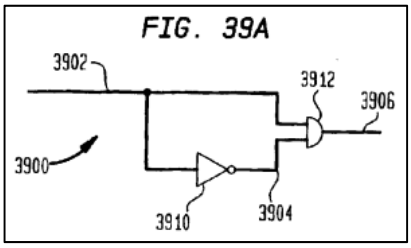
D. "pulse shaping means for shaping a string of pulses from a reference signal" ('508 patent, claim 1)

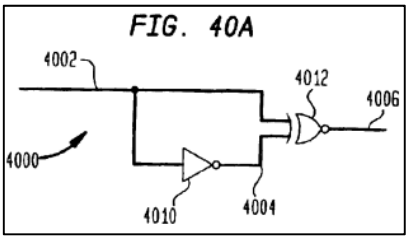
Intel's Proposed Construction	PV's Proposed Construction
Function: shaping a string of pulses from a reference signal **Structure**: the pulse shaping circuit 3900	**Function:** shaping a string of pulses from a reference signal **Structure:** pulse shaper 3900 in Fig. 39A; pulse

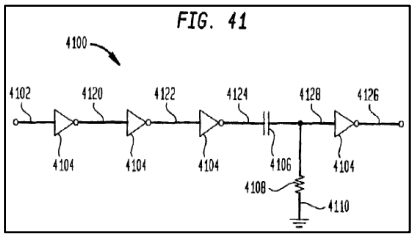
Intel's Proposed Construction	PV's Proposed Construction
shown in Fig. 39A and described at 48:8-39, the pulse shaping circuit 4000 shown in Fig. 40A and described at 48:40-49:5, and the pulse shaping circuit 4100 shown in Fig. 41 and described at 49:6-26, which incorporates circuit element 4104 shown in Fig. 43 and described at 49:6-26; and equivalents thereof.[19]	shaping circuit/pulse shaper 4000 in Fig. 40A; pulse shaping circuit 4100 in Fig. 41; harmonic enhancement module 4602 in Fig. 46; signal shaper 5010 in Fig. 50; harmonic enhancement module 5124 in Fig. 51B-C; pulse shaper 5310 in Fig. 53; pulse shaper 5438 in Fig. 54A; pulse shaper 5438 in Fig. 55; pulse shaper 5632 in Fig. 56; pulse shaping circuit 5722 in Fig. 57A-C, pulse shaper 6216 in Fig. 62; pulse shaper 7812 in Fig. 78; and equivalents

The parties dispute whether the construction should identify specific structures that perform the claimed function (as Intel proposes), or whether the structures can include empty "black boxes" that encompass any circuitry that performs the function (as PV proposes).

Intel's Proposal. Claim 1 of the '508 patent recites "[a]n apparatus for frequency up-conversion comprising: ***pulse shaping means*** for ***shaping a string of pulses from a reference signal***." Section 4 of the '508 specification is entitled "Harmonic Enhancement," which the patent states "may also be called 'pulse shaping'" because the purpose of harmonic enhancement is to "shape the oscillating signal 2804 into a string of pulses of a desired pulse width." '508, 45:31-33. The patent states that it discloses "three" pulse-shaping circuits: (1) pulse shaping circuit 3900 in Figure 39A; (2) pulse shaping circuit 4000 in Figure 40A; and (3) pulse shaping circuit 4100 in Figure 41.







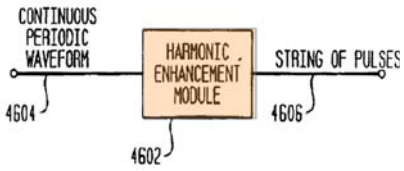
Id., 45:31-43. Each figure clearly discloses (and is described in the specification as disclosing) a combination of specific components (such as inverters, AND gates, NOR gates, resistors, and

[19] Intel has revised its construction to make clear that Figure 41 incorporates circuit element 4104 shown in Figure 43. The substance of Intel's proposed construction remains the same.

capacitors) arranged in a specific configuration to shape oscillating signals into a string of pulses. *Id.*, 48:8-49:26. The patent does not disclose any other structures that perform the claimed function of "shaping a string of pulses from a reference signal" and should be limited to these structures and their equivalents. *Noah Sys.*, 675 F.3d at 1318.[20]

PV's Proposal. PV impermissibly attempts to broaden the claim by including empty "black box" structures that disclose no specific circuitry and are described in the patent solely in functional terms. For example, PV points to the empty "harmonic enhancement module 4602" (orange) (also described as "pulse shaping circuit 4602") shown in Figure 46, which the patent describes only as "shap[ing]" "a continuous and periodic waveform 4604 into a string of pulses 4606." '508, 45:59-65.

FIG. 46



PV similarly points to empty boxes such as pulse shaper 5632 in Figure 56 for which the patent only provides a similar functional description. '508, 61:2-4 ("The oscillating signal is shaped by pulse shaper 5632 and a string of pulses 5634 is created."). These empty boxes provide no indication *of the structure* that performs the claimed function. Nor does the specification provide any description of what structure is inside these generic boxes, instead describing them only in terms of their function.[21] VDW ¶¶ 144-150. By including these black boxes, PV improperly attempts to cover ***any*** circuit

[20] PV argues that Intel allegedly "improperly" omits column 46:65-47:7, 47:26-35, 47:45-52 (Pl. Op. 45), but these passages refer only to empty "black boxes" and the functions they perform, not specific structure for performing the required function.

[21] PV argues that "harmonic enhancement module 4602" has sufficient structure because the patent says the module has "digital logic devices." Pl. Op. 45 (quoting '508, 47:3-6, 30-34). But "digital logic devices" are ***themselves*** generic structures, and the patent thus provides no definite structure for the harmonic enhancement module. VDW ¶ 149.

configuration that can achieve the claimed function. *Metter-Toledo*, 671 F.3d at 1295-96.

The fundamental bargain of means-plus-function claiming is that the patentee gets the benefit of functional claiming in exchange for limiting the claim scope to the specific structures disclosed in the specification for performing the function. *Noah*, 675 F.3d at 1318; *O'Reilly v. Morse*, 56 U.S. 62, 120 (1853). PV may not do an end-run around this requirement by pointing to empty boxes described as performing a function and then seeking to cover any structures that perform the function. In *Mettler–Toledo*, 671 F.3d 1291, for instance, the patent disclosed both a generic analog-to-digital converter in a patent figure and a specific analog-to-digital converter in another figure, but the court limited the claim term to the specifically disclosed structure: "[i]f a patentee chooses to disclose a single embodiment, then any means-plus-function claim limitation will be limited to the single disclosed structure and equivalents thereof." *Id.* at 1295-96; *J & M Corp. v. Harley-Davidson, Inc.*, 269 F.3d 1360, 1367 (Fed. Cir. 2001) ("The literal scope of a properly construed means-plus-function limitation does not extend to all means for performing a certain function. Rather, ***the scope of such claim language is sharply limited to the structure disclosed in the specification and its equivalents***.").

E. "aperture generation means … for generating a string of multiple pulses from said string of pulses" ('508 patent, claim 1)

Intel's Proposed Construction	PV's Proposed Construction
Function: generating a string of multiple pulses from said string of pulses **Structure**: the aperture generation module 7806 shown in Fig. 79 and described at 49:54-50:5; and equivalents thereof.	**Function:** generating a string of multiple pulses from said string of pulses **Structure:** aperture generation module 7806 in Fig. 78 having gate(s) and delay(s) such as the aperture generation module shown in Fig. 79; and equivalents thereof

The parties agree that the required structure for this term includes the "aperture generation module" 7806 shown in Figure 79. The dispute is whether the structure should also include the aperture generation module 7806 in *Figure 78* which is an empty black box without any disclosure of the

structure inside (as PV proposes).

Intel's Proposal. There is no dispute that "aperture generation module 7806" performs the required function of "generating a string of multiple pulses from said string of pulses." The only actual structure disclosed for aperture generation module 7806 is in Figure 79 (reproduced below).

FIG. 79

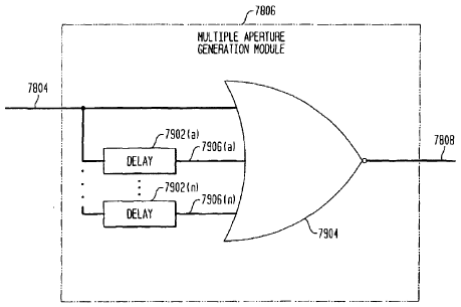
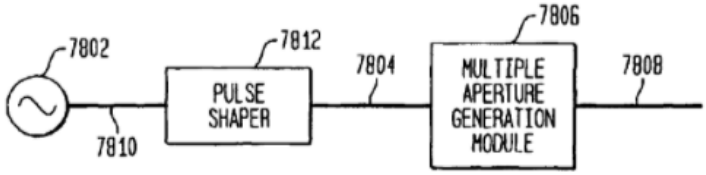


Figure 79 shows aperture generation module 7806 as including multiple "delay" components 7902 and a "NOR" gate 7904. *Id.*, 49:54-50:5. No other figure in the specification shows the structure of an aperture generation module, and the corresponding structure for this term is therefore the aperture generation module 7806 shown in Figure 79 and described at 49:54-50:5.[22]

PV's Proposal. PV incorrectly attempts to broaden the claim by including in the construction a "black box" containing no structure whatsoever—multiple aperture generation module 7806 in Figure 78 (shown below):

FIG. 78



[22] The specification excerpt (49:37-53) that PV says was improperly excluded from Intel's construction does not belong in the construction. As PV admits, that excerpt describes "the type of signal that needs to be processed by the aperture generation means," not a structure of the aperture generation means. Pl. Op. 47.

The patent never discloses any structure for aperture generation module 7806 in Figure 78, and it therefore cannot be included in the construction for the same reasons discussed in the prior term.

PV's rationale for including the empty box in Figure 78 shows why it is improper. PV states that Figure 79 is merely "one exemplary configuration" of aperture generation module 7806 and that the term should be defined more generally to cover ***any*** structures that contain "gate(s) and delay(s) that performs the recited function." Pl. Op. 46. But that is precisely what § 112 ¶ 6 does ***not*** allow. *Mettler-Toledo*, 671 F.3d at 1295-96. Indeed, confirming this, PV itself agreed to Intel's proposed construction in prior litigation. Ex. 5 (*ParkerVision, Inc. v. Qualcomm*, No. 6:14-cv-687, D.I. 124 (M.D. Fla. May 1, 2015)).

F. "generating a string of multiple pulses from said string of pulses" ('508 patent, claim 1)

Proposed Constructions
Intel: "generating a signal with multiple the number of pulses as said string of pulses"
PV: Plain and ordinary meaning

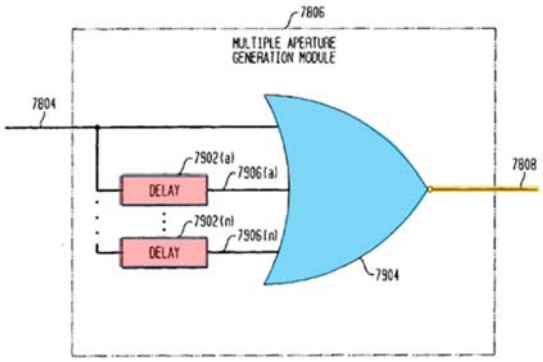
The parties dispute whether this term should be construed in accordance with the claims and specification—as "generating a signal with ***multiple the number of pulses*** as said string of pulses" (as Intel proposes)—or whether it should be given a purported "plain and ordinary" meaning that would render claim language meaningless (as PV proposes).

Intel's Proposal. Claim 1 of the '508 patent recites an "apparatus for frequency up-conversion" that includes, among other things, a "pulse shaping means" and an "aperture generation means." The claim requires the pulse shaping means to "shap[e] ***a string of pulses*** from a reference signal," and requires the "aperture generation means" to then "generat[e] ***a string of multiple pulses from said string of pulses***." The claim language thus makes clear that the term at issue here—the "string of ***multiple*** pulses" generated by the aperture generation means—is something ***different*** from

the "string of pulses" that is produced by the pulse shaping means. The claim language also makes clear that the difference between the two strings of pulses is the "***multiple***" number of pulses that the aperture generation means generates from the pulses received from the pulse shaping means. *Comaper Corp. v. Antec, Inc.*, 596 F.3d 1343, 1348 (Fed. Cir. 2010) (terms "drive bay" and "drive bay slot" not synonymous as "two different terms used in a patent have different meanings").

The specification confirms that the purpose of the aperture generation module is to generate ***more pulses than it received*** in order to increase the amplitude of the desired harmonic. The patent explains that the aperture generation module (shown in Fig. 79, below) uses four different delay modules (red), each of which receives the string of pulses and delays the pulses in that string by different periods of time:

FIG. 79

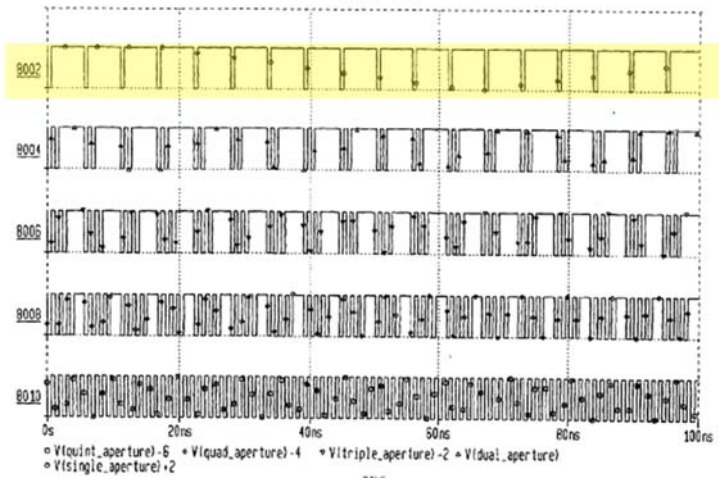


'508, Fig. 79, 49:54-50:5. The patent explains that a NOR gate (blue) then combines the original string of pulses with each of the four delayed strings of pulses to create a "string of ***multiple*** pulses" (7808, orange). *Id.*, 49:54-50:5. The result is that the string of multiple pulses has a pulse at every point in time that the original string had a pulse ***and*** a pulse at every point in time that the delayed strings have: "When string of pulses 7804 and first through nth delayed strings of pulses 7906(a)-7906(n) are combined by 'NOR' gate 7904, ***string of multiple pulses 7808 is created <u>having n+1 pulses</u> for every cycle of string of pulses 7804***." *Id.*, 50:1-5. The aperture generation means thus generates a signal with

multiple pulses per pulse received in the original string of pulses. The term should therefore be construed as "generating a signal with multiple the number of pulses as said string of pulses." *Ormco Corp. v. Align Tech., Inc.*, 498 F.3d 1307, 1313 (Fed. Cir. 2007) (court should construe term in way that "aligns with the patent's description of the invention" (quotation marks omitted)).

PV argues (Pl. Op. 56-57) that Intel's proposed construction excludes an embodiment—pulse train 8002 in Figure 80 (below)—but this figure actually confirms that Intel's construction is correct.

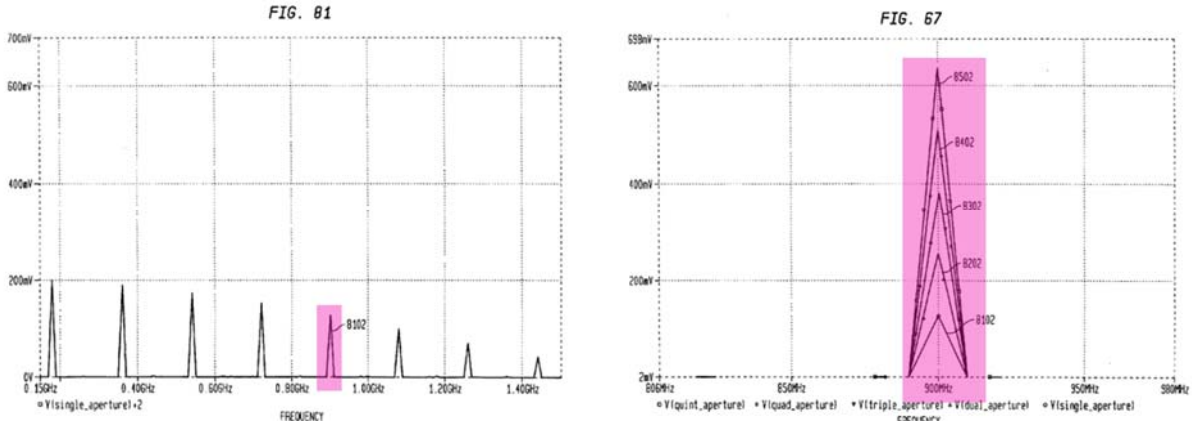
FIG. 80



It is true that pulse train 8002 (shown in yellow above) has only "one pulse for each pulse of the string of pulses." Pl Op. 56;'508, 50:6-7 ("FIG. 80 illustrates a pulse train 8002 that is one pulse per cycle of string of pulses 7804."). But pulse train 8002 is ***not*** described as an embodiment of the patented invention. It is instead the point of reference against which the embodiments of the invention—which do use multiple pulses per cycle—are compared. After showing pulse train 8002, Figure 80 shows pulse trains 8004, 8006, 8008, and 8010, each of which has multiple pulses per cycle of the received string of pulses (*id.*, 50:7-22), and the patent then immediately elaborates on "the advantages of using multiple apertures per cycle" (*id.*, 50:23-24).

According to the patent, the purpose of the claimed invention—to increase the amplitude of the desired harmonic relative to the other harmonics—is shown by comparing Figure 81 with Figure

67. In Figure 81 (without the multiple aperture generation module), the amplitude (8102) of the desired harmonic at 900 MHz signal is small and similar to the amplitudes of the other undesired harmonics. In Figure 67, with multiple the number of pulses, the desired harmonic has a much higher amplitude than it did without the extra pulses (compare 8502 to 8102).



Compare id., Fig. 67, *with id.*, Figs. 81, 82, 83, 65, 66. The patent explains that, "[a]s can be seen, the desired harmonic amplitude is increased and the undesired harmonics decreased as a function of the number of pulses per cycle." *Id.*, 50:37-40. This is what purportedly eliminates the need for an "elaborate filter" to extract the desired frequency. If the claim were construed to cover pulse train 8002 which has only "one pulse for each pulse of the string of pulses," both the input and output of the claimed aperture generation means would be identical, meaning that rather than strengthen the desired harmonic, this claim element would have no impact on the up-conversion apparatus of claim 1. Thus, far from undermining Intel's construction, pulse train 8002 reinforces that the claimed invention requires multiple pulses per cycle of the received string of pulses.

PV's Proposal. PV's "plain and ordinary meaning" construction—which PV suggests would allow the term to cover a string of pulses having only ***one*** pulse per cycle of the received string of pulses (Pl. Op. 56)—should be rejected. ***First***, PV's proposal is inconsistent with the claim language. The claim recites two strings: a "string of pulses" and a "string of ***multiple*** pulses." '508, Cl 1. Those

two different terms are presumed to mean two different things, and the word "multiple" must be given meaning. PV violates these basic principles by allowing both terms to mean the same thing, i.e., interpreting both strings to merely require more than one pulse. *Bicon, Inc. v. Straumann Co.*, 441 F.3d 945, 951 (Fed. Cir. 2006) ("claim language should not [be] treated as meaningless" and rejecting construction that would "read limitations … out of the claim"). ***Second***, PV's proposal is contrary to the specification's clear disclosure of the invention as requiring a "string of multiple pulses" that has ***multiple*** the number of pulses for every cycle of the "string of pulses" in order to increase the amplitude of the desired harmonic. '508, 49:61-50:5 ("string of multiple pulses 7808 is created having ***n+1 pulses*** for every cycle of string of pulses 7804").

G. "gating means for gating a bias signal under the control of said string of multiple pulses to generate a periodic signal having a plurality of harmonics at least one of which is at a desired frequency" ('508 patent, claim 1)

Intel's Proposed Construction	PV's Proposed Construction
Function: gating a bias signal under the control of said string of multiple pulses to generate a periodic signal having a plurality of harmonics at least one of which is at a desired frequency **Structure**: switch 2816 shown in Fig. 28A and described at 35:14-36:24 and 45:47-46:37; GaAsFET 2901 shown in Fig. 29A and described at 36:25-50; GaAsFETs 3002 and 3004 shown in Fig. 30A and described at 36:25-50; switch 5312 shown in Fig. 53 and described at 58:63-59:13, switch 5636 shown in Fig. 56 and described at 60:66-61:10; switch 5420 shown in Fig. 54A and described at 60:1-22; switch 5724 shown in Figs. 57A-B and described at 65:49-55; and equivalents thereof.[23]	**Function:** gating a bias signal under the control of said string of multiple pulses to generate a periodic signal having a plurality of harmonics at least one of which is at a desired frequency **Structure:** the switches shown in Fig. 28A, 29A, 30A, 31A, 32A, 33A, 53, 54A, 55, 56, 57A-C; and equivalents thereof

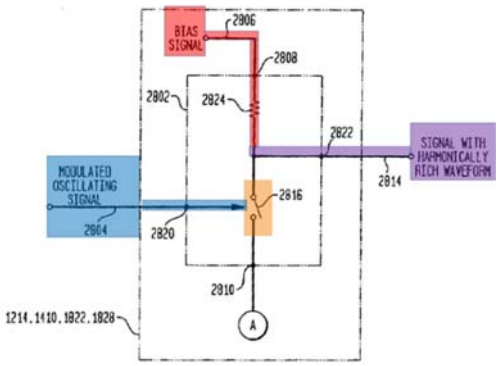
The parties dispute whether the corresponding structure can include structures that do ***not*** gate

[23] PV's original construction included "the ***structures*** shown in Fig. 28A, 29A, 30A, 31A, 32A, 33A, 53, 54A, 55, 56, 57A-C; and equivalents thereof." PV's construction now covers only "the ***switches***" in those figures. Intel agrees that the ***specific "switches"*** shown in Figures 53, 54A, 56, and 57A-B are corresponding structure and has revised its construction accordingly.

a ***bias*** signal (as PV proposes).

Intel's Proposal. Claim 1 of the '508 patent recites an apparatus for frequency up-conversion that comprises, among other things, a "gating means" for "[1] gating a bias signal [2] under the control of said string of multiple pulses [3] to generate a periodic signal having a plurality of harmonics at least one of which is at a desired frequency." Consistent with Intel's proposed construction, the patent specifically identifies the switches and GaAsFETs in Figures 28A, 29A, and 30A as performing the claimed function. For example, in describing Figure 28A (below), the patent explains that a "bias signal 2806 is applied to the first input 2808" of switch module 2802, which is "comprised of … ***a switch 2816 (orange)***," *id.*, 35:17-18. The patent further states that "[a] modulated oscillating signal 2804 is connected to the control input 2820," *id.*, 35:29-30, and "[t]he harmonically rich signal 2814 … is found at the output 2822," *id.*, 35:41-43). Thus, the switch performs the gating function in the claim.

FIG. 28A



The same is true for the switches in Figures 53, 56, 54A, and 57A-B. For instance, the patent states that "[i]n the FM and PM embodiments … [a] string of pulses 5311 controls the opening and closing of the ***switch 5312***," which is connected through resistor 5330 to a bias signal. *Id.*, 58:66-59:6; *id.*, 59:4-6. The patent then explains that "[t]he ***output of switch 5312*** is a harmonically rich signal 5316." *Id.*, 59:15-16; *see also* 60:1-22; 65:49-55 (similar description for switches in Fig. 54A and Figs. 57A-B). The patent does not describe any other corresponding structures.

PV's Proposal. PV's proposed construction includes additional figures that do not perform the claimed function of gating a bias signal. PV points to Figures 31A, 32A, 33A, 55, and 57C (Pl. Op. 49-50)—but these figures ***do not gate a bias signal***:

- Figures 31A, 32A, and 33A show gating a "***reference signal***" instead of a "bias signal."
- Figure 55 shows a "bias signal" and an "information signal" that are combined to create a "reference signal." *Id.,* Fig. 55, 60:29-31 ("Reference signal 5506 is generated when information signal 5450 and bias signal 5422 are combined by a summing module 5504."). The ***reference signal*** 5506—not the bias signal 5422—is gated under the control of the string of pulses 5440 to generate the harmonically rich signal 5508. *Id.*, 60:24-29.
- Similarly, Figure 57C shows a bias signal 5716 and an information signal 5702 that are combined by summing module 5740. *Id.*, Fig. 57. The ***signal generated by summing module*** (i.e., signal 5742)—not the "bias signal"—is gated under the control of string of pulses 5706 to generate harmonically rich signal 5708. *Id.*, Fig. 57C, 70:15-17.

The patent specifically distinguishes between gating a bias signal, on the one hand, from gating the reference or information signal on the other. *Id.*, Abstract ("When the invention is being used in the frequency modulation (FM) or phase modulation (PM) implementations, the oscillating signal … ***causes the switch to gate the bias signal***. In the amplitude modulation implementation (AM), the oscillating signal … ***causes the switch to gate a reference signal*** that is substantially equal to or proportional to the information signal."). These figures therefore are not corresponding structures because the specification does not "link" any of those structures to the function ("gating a bias signal") recited in the claim. *MobileMedia Ideas LLC v. Apple Inc.*, 780 F.3d 1159, 1169-70 (Fed. Cir. 2015).

H. "gating" ('508 patent, claim 1)

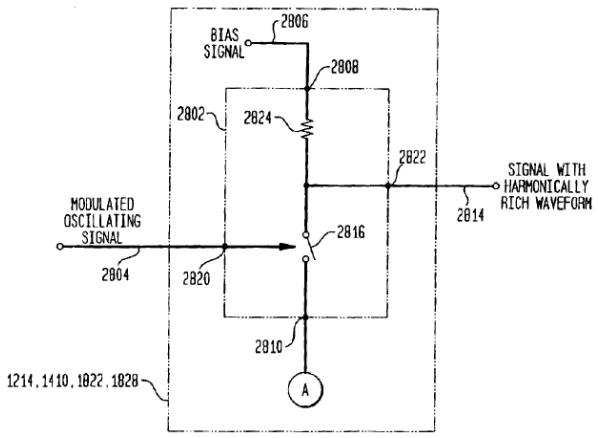
Proposed Constructions
Intel: "opening and closing a device to selectively output a signal" **PV**: "changing between the open and closed states of a switch, as dictated by an independent control input"

The parties' primary dispute centers on whether the term "gating" should be construed consistent with its use in the specification as "opening and closing a device to selectively output a signal" (as Intel proposes), or whether the term should be limited to a particular type of switch that

opens and closes as dictated by "an independent control input" (as PV proposes).

Intel's Proposal. The '508 patent explains that "gating" refers to the opening and closing of a device, such as a switch, in order to selectively allow a signal to pass through. For example, in Figure 28A below, an oscillating signal 2804 opens and closes a switch, which allows the bias signal 2806 to be either output at 2822 (if the switch is open) or not output (if the switch is closed). '508, 35:63-66 ("When the switch 2816 is 'open,' the output 2822 of switch module 2802 is at substantially the same voltage level as bias signal 2806.").

FIG. 28A



The patent refers to this opening and closing of the switch as "gating" the bias signal. '508, 34:34-35 ("A bias signal 2806 is gated as a result of the application of a modulated oscillating signal 2804 …."). This use of gating—as involving the opening and closing of a switch to selectively output a signal—is consistent throughout the '508 patent. *Id.*, 44:18-42 ("The objective is for the switch to ***close and open*** such that the bias/reference signal is 'crisply' ***gated***"), 24:36-25:4 ("[A]n oscillating signal 1612 is generated by local oscillator 1610 … and … ***switch module 1614 gates*** the reference voltage 1608 at a rate that is a function of the oscillating signal 1612."), Abstract (describing gating the bias versus the reference or information signal), 2:38-40, 37:17-18. Intel's proposed construction—"opening and closing a device to selectively output a signal"—thus precisely matches the patent's use of the term

"gating" and is consistent with the use of the term "gating" in the prior art. VDW ¶ 151-153.

PV incorrectly argues that Intel's proposed construction "improperly sets forth a purpose of 'gating'" that is different from the purpose provided in claim 1. Pl. Op. 52-53. But Intel's construction does not set forth a "purpose" of "gating." Instead it describes ***what*** gating is—i.e., opening and closing a device to selectively output a signal—precisely as the term is described in the patent. The claim separately identifies the purpose of the "gating means" required by this specific claim—namely, "to generate a periodic signal having a plurality of harmonics." PV also argues that Intel's construction should be rejected because "it is unclear what it means for a switch to '*selectively* output a signal.'" Pl. Op. 53. But PV's brief states that it understands "selectively" to refer to "outputting a signal only when the switch is ON (closed)." *Id.*

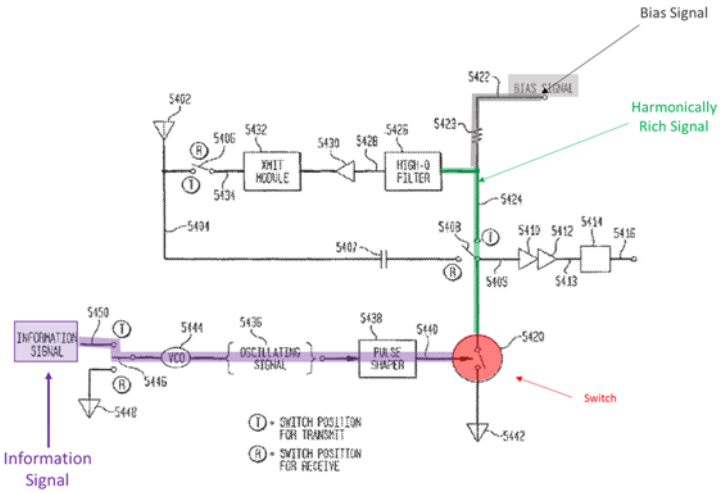
PV's Proposal. PV incorrectly asserts that "gating" must be limited to only a particular device (a switch), must involve "changing between the open and closed states of a switch," and must be "dictated by an independent control input." There is no basis in the patent for these limitations. ***First***, PV is wrong that the general term "gating" is limited to a switch and that the switch's opening and closing must be "dictated by an independent control signal." There is no basis in the patent to limit "gating" to the opening and closing of a switch as "dictated by an independent control signal." Indeed, the patent never even uses the phrase "independent control input." Moreover, the patent makes clear that the gating could be accomplished by diodes—two-terminal devices that do not have any particular "control input," much less "an independent control input" (whatever that means). '508, 49:21-23; '551, 56:60-68, 99:40-55, Figs. 28C, 28D, 66C, 66D; VDW ¶ 153. ***Second***, PV argues that "gating is not merely the opening and closing of a device" but rather "is the process of *changing* between these two states i.e., between open and closed." Pl. Op. 52. PV fails to explain the distinction or cite to any support for this language in its construction.

I. "bias signal" ('508 patent, claim 1; '108 patent, claim 1)

Proposed Constructions
Intel: "a signal having a fixed voltage or fixed current" **PV**: "1) a signal having a steady, predetermined level; or 2) the modulating baseband signal"

The parties agree that a "bias signal" refers to a signal having a "steady" or "fixed" voltage or current. The parties' dispute is whether the term "bias signal" can also include the opposite—a "modulating baseband signal," which is neither steady nor fixed (as PV proposes).

Intel's Proposal. In the '108 and '508 patents, a "bias signal" is described as a fixed voltage or current used to set the level of another signal (i.e., to "bias" the other signal in a particular manner). '508, 34:34-60 ("The bias signal 2806 is generally a fixed voltage."), 33:22-23; '108, 32:54-67, 31:3-4. As explained in the patents, the bias signal sets the amplitude of the harmonically rich signal output from the switch. This is shown in the frequency and phase modulation modes shown in Figure 54A and 54B, which have been combined and annotated as shown below



'108, Figs. 54A, 54B. As shown, an information signal is first used to modulate the frequency or phase of an oscillating signal to create a modulated oscillating signal 5436. Based on that signal, switch 5420 generates harmonically rich signal 5424. When switch 5420 is on (closed), the value of the output

signal is at ground 5442. When switch 5420 is off (open), the value of the output signal is at the value of the bias signal 5422. *Id.*, 55:5-25. This fluctuation between the amplitude of the bias signal and the amplitude of ground (zero) results in the harmonically rich signal. *Id.* The fixed bias signal is thus used to set the amplitude of the generated signal.

This is also shown in the amplitude modulation mode of Figure 55. In Figure 55, the bias signal 5422 is first combined with information signal 5450 to create reference signal 5506. When switch 5420 is on (closed), the value of the output signal is at ground 5442. When switch 5420 is off (open), the value the output signal is at the value of the reference signal 5506. *Id.*, 55:5-34. Thus, the fixed bias signal is used to form the reference signal which is then used to set the amplitude of the harmonically rich signal 5500 generated by the switch. *Id.*

In all embodiments, the bias signal has a fixed level and is described as having either a fixed voltage or fixed current (depending on the embodiment). '108, 56:1-27 ("In the FM and PM modulation modes, bias/reference signal 5646 is referred to as a bias signal 5646, and it is substantially non-varying.").; *Id.,* 54:3-29; '108 patent, 31:3-4; '508, 33:22-23 ("The bias signal 2704 is usually a direct current (DC) signal."; VDW ¶¶154-157 (a DC signal has either a fixed current or fixed voltage). The patents' use of the term is consistent with the use of the term "bias" in the art. Ex. 6 (The Illustrated Dictionary of Electronics, 7th Ed. 1997) ("Bias current: A ***steady, constant current*** that presets the operating threshold or operating point of a circuit or device, such as a transistor, diode, or magnetic amplifier."). Indeed, the bias signal must be fixed in order to serve its purpose of helping to create the harmonically rich signal. VDW ¶ 155.

PV argues that the specifications state only that the bias signal is "generally" a fixed voltage and does not always have to be a fixed voltage. Pl. Op. 54. But Intel's proposed construction does not require it to always be a fixed ***voltage.*** Consistent with the specification, Intel's proposed construction

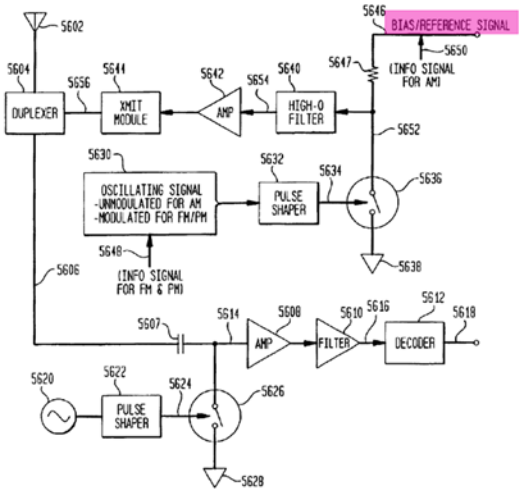
also states that "bias signal" could refer to a fixed ***current***, which explains the specifications' use of the word "generally." In every instance that a "bias signal" is described, the "bias signal" is either a fixed voltage or a fixed current.

PV's Proposal. PV incorrectly seeks to broaden "bias signal" to encompass the opposite concept of a signal that is ***not*** fixed—i.e., to include "the modulating baseband signal." This finds no support in the intrinsic evidence. The '108 and '508 patents never describe the "bias signal" as including a "modulating baseband signal." Nor do the specifications ever define "baseband signal" to include a "bias signal"—they are instead different signals with different purposes. '108, 7:44-48 (defining "baseband signal" as "[a]ny generic information signal desired for transmission and/or reception," and stating that "baseband signal" refers to "the information signal that is generated at a source prior to any transmission (also referred to as the modulating baseband signal)"; '508, 9:5-11.

PV points to a single sentence from the specifications' description of Figure 56 in an attempt to support its construction, but PV takes the sentence out of context. Pl. Op. 53-54. Figure 56 (below) shows a combination of the phase/frequency modulation mode and the amplitude modulation mode. To capture these separate embodiments, the figure refers to a "bias/reference signal 5646":

FIG. 56

TRANSMITTER USING PRESENT INVENTION IN FULL DUPLEX COMMUNICATIONS CIRCUIT WITH UNIVERSAL FREQUENCY DOWN-CONVERTER



The "bias/reference signal 5646" refers to two different signals that are used depending on the mode of operation. The patents explain that, in the frequency and phase (FM and PM) modulation modes of operation, when the information signal is modulated onto the oscillating signal, the "bias signal" is used to set the amplitude of the harmonically rich signal created by the switch. '508, 61:7-10. The patents further explain that, in the amplitude (AM) modulation mode, the information signal is combined with the bias signal to create a "reference signal," and the reference signal is then used to set the amplitude of the harmonically rich signal created by the switch. *Id.*, 61:8-13. Thus, depending on the mode of operation, the circuit uses either the bias signal ***or*** the reference signal. The "bias/reference signal 5646" term in the figure refers to the two different signals—the bias signal and the reference signal—used in the different modes.

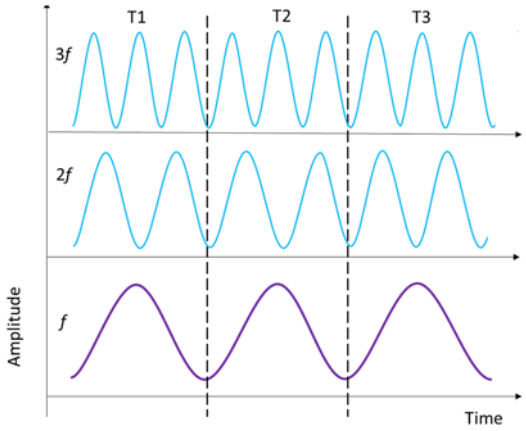
PV pulls out the following sentence from the discussion of Figure 56's amplitude mode as support for its proposed assertion that the bias signal need not be fixed: "It is well known to those skilled in the relevant art(s) that the information signal 5650 may be used as the bias/reference signal 5646 directly without being summed with a bias signal." *Id.,* 61:14-17. PV argues that this sentence indicates the information signal can be used as the "bias signal." That takes the sentence entirely out of context. This sentence is clearly referring to the AM mode—a mode in which, as explained above, "bias/reference signal 5646" is a ***reference*** signal. In this particular embodiment of the AM mode, the "reference signal" is not the summation of the information signal and a bias signal; instead, the information signal alone is used as the "reference signal." *Id.*, 2:39-43. But nothing in the sentence or elsewhere in the patents says that the information signal can be used as the "bias signal." It would make no sense to use an information signal as a bias signal because it is the information signal that is supposed to be biased. VDW ¶¶ 155-157. Indeed, if PV's construction were adopted, the sentence PV relies on would be rendered nonsensical. It would read: "the information signal [] may be used as the

bias signal directly without being summed with a *bias signal*."[24]

IV. '108 Patent Overview

The '108 patent is directed to a specific apparatus and method for accomplishing frequency up-conversion in wireless devices. The patent acknowledges that multiple techniques to up-convert signals to high-frequency signals for wireless transmission were well known before the claimed invention. '108, 14:1-6; VDW ¶ 116-18. The patent asserts, however, that such techniques were costly and wasted power because they relied on multiple expensive components, including high-frequency oscillators, to upconvert. '108, 14:1-6.

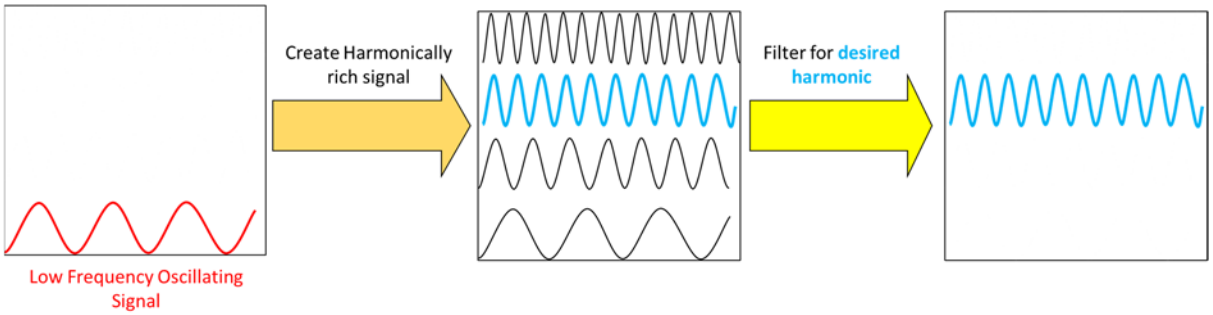
The patent purports to solve this problem with an allegedly novel system for up-converting that avoids the use of such expensive components because it up-converts by generating what is called a "harmonically rich signal." *Id.,* 2:19-22, 2:31-35. As Fourier discovered in the 1800s, all signals are comprised of components called "harmonics." *Id.*, 39:63-65. "Harmonics" are signals within a signal that have frequencies that are integer multiples of the original signal. *Id.*, 39:65-40:1. As shown below, if the original signal has a frequency of *f*, its harmonics have frequencies of 2*f*, 3*f*, etc.



[24] PV's construction is also inconsistent with dependent claim 2 of the '108 patent, which makes clear that a bias signal, an information signal, and a reference signal are different things. Claim 2 recites a "combining module" that "receive[s] the bias signal and an information signal" and "output[s] a reference signal." '108, Cl. 2. Under PV's proposed construction, claim 2 would make no sense because the bias signal could be an information signal.

VDW ¶ 108. A harmonically rich signal is one that includes multiple harmonics. '108, 17:15-24. Certain waveforms, like a sinusoidal wave, may have only one frequency component—at the "fundamental frequency" of the waveform—and no harmonics. *Id.*, 40:6-13. Other waveforms, like a square wave, have multiple harmonics, each of which is a representation of the original signal but at a higher frequency. Such waveforms are said to be harmonically rich. *Id.*, 40:24-47.

The '108 patent teaches that a cheaper, low-frequency oscillator can be used to perform up-conversion in a two-step process. ***First***, the oscillator generates a low-frequency control signal that controls the opening and closing of a switch, which outputs a harmonically rich signal consisting of a series of harmonics—2x, 3x, 4x, etc. the frequency of the oscillating signal. *Id.*, 2:19-23 (Summary of Invention) ("As a result of this opening and closing, a signal that is harmonically rich is produced with each harmonic of the harmonically rich signal being modulated substantially the same as the modulated intermediate signal."), 2:31-38. ***Second***, a filter selects one of those higher-frequency harmonics as the desired up-converted signal. *Id.*, Abstract ("In both embodiments, the output of the switch is filtered, and the desired harmonic is output."). Because the selected harmonic is a representation of the original signal but at a higher frequency, the system performs up-conversion by simply selecting the desired harmonic and filtering out the remaining unwanted harmonics. *Id.*, 2:19-24, 2:31-41.



VDW ¶ 120. Thus, a specific control signal is used to control a switch to generate the desired harmonically rich signal (from which the desired harmonic is selected). The control signal is a ***sub-***

harmonic of and ***lower-frequency signal*** than the desired output frequency. '108, Abstract ("[t]he frequency of the oscillating signal being selected as a ***sub-harmonic*** of the desired output frequency."), 61:58-60 ("The frequency of the oscillating signal 5704, 5738, 5744 must be a ***subharmonic*** of the frequency of the desired transmission signal 5714."). As explained above, a sub-harmonic is an integer *sub*multiple of the fundamental frequency. *Id.*, 9:23-34. By using a control signal that is a sub-harmonic of the desired output frequency, the switch generates a signal with multiple harmonics of the original signal (i.e., representations of the original signal but at higher frequencies). *Id.*, 52:2-9; 61:42-62. The patent explains that each of these harmonics carry the same information as the original signal and, thus, are just an up-converted version of the original signal: "***As the harmonics have frequencies that are integer multiples of the repetition frequency of signal 1908***, and since they have the same information content as signal 1908 (as just stated), ***the harmonics each represent an up-converted representation of signal 1908***." *Id.,* 16:24-28. The system can then select one of those harmonics—a higher-frequency representation of the original signal—to use as the desired output signal. *Id*, Abstract ("[T]he output of the switch is filtered, and the desired harmonic is output.").

Thus, the '108 patent purports to teach a method of up-conversion without the use of a high-frequency oscillator and other expensive components but instead using a low-frequency oscillator to generate higher-frequency harmonics and filtering for the harmonic with the desired frequency: "Because it up-converts frequency, ***the present invention can take advantage of the relatively low cost of low frequency oscillators*** to generate stable, high frequency signals." *Id.*, 9:55-58.

A. "control signal" ('108 patent, claim 1)

Proposed Constructions
Intel: "an oscillating signal that controls the first switch with a frequency that is a sub-harmonic of and lower than the desired output frequency" **PV:** Plain and ordinary meaning

The parties' dispute is whether the term "control signal" should be construed consistent with the control signal disclosed in the patent (as Intel proposes) or instead, to encompass virtually any generic control signal (as PV proposes).

Intel's Proposal. As reflected in the '108 patent's title "Method and System for Frequency Up-conversion," the '108 patent claims are all directed to up-converting using a "frequency conversion module." '108, Cl. 1. The patent describes that, to perform this allegedly novel up-conversion, the "frequency conversion module" uses a particular type of control signal to control a switch that up-converts: "a first switch ***configured to up-convert a signal based on a control signal*** and a bias signal."

The patent asserts that prior known methods of up-conversion required the use of costly and inefficient components such as high-frequency oscillators which produce high-frequency signals. *Id.,* 14:1-6 ("Typically…upconverting the information signal to broadcast frequency requires, at least, filters, amplifiers, and frequency multipliers. Each of these components is costly, not only in terms of the purchase price of the component, but also because of the power required to operate them."); VDW ¶ 117 (a frequency multiplier is used to produce a high-frequency signal). The patent purports to address this problem—and avoid the use of such inefficient and expensive components—by up-converting using a specific control signal that controls a switch to generate a harmonically rich signal. '108 patent, 2:19-23 ("As a result of this opening and closing, a signal that is harmonically rich is produced with each harmonic of the harmonically rich signal being modulated substantially the same as the modulated intermediate signal."), 2:31-38.

As described above, a harmonically rich signal is made up of harmonics—representations of the original signal at frequencies that are integer multiples of the original signal. *Id.* Specifically, as the patent explains, each of the harmonics in the harmonically rich signal represents an up-converted (i.e. higher frequency) representation of the original signal:

> ***As the harmonics have frequencies that are integer multiples of the repetition frequency of signal 1908***, and since they have the same information content as signal 1908 (as just stated), ***the harmonics each represent an up-converted representation of signal 1908***.

Id., 16:24-28. The patent explains that the system can upconvert by simply selecting one of the harmonics (from the harmonically rich signal generated by the switch) as the desired upconverted signal and filtering out the rest. *Id.*, Abstract ("In both embodiments, the output of the switch is filtered, and the desired harmonic is output.").

For the switch to produce the desired harmonically rich signal that includes the desired harmonic that constitutes the up-converted signal, the patent explains that a particular type of control signal is required: the control signal must be selected based on the desired frequency of the signal to be transmitted. Specifically, the patent explains that the claimed up-conversion requires a control signal that is a sub-harmonic of and lower than the desired output frequency:

> A method and system is described wherein a signal with a lower frequency is up-converted to a higher frequency. … ***The up-conversion is accomplished by controlling a switch with an oscillating signal, the frequency of the oscillating signal being selected as a sub-harmonic of the desired output frequency.*** … In both embodiments, ***the output of the switch is filtered, and the desired harmonic is output***."

Id., Abstract. The control signal must be a sub-harmonic of and lower than the desired output frequency because that is what enables the system to generate the desired harmonic—the up-converted representation of the original signal—which is then selected and transmitted.

Consistent with this, every embodiment in the '108 patent up-converts by using a control signal to control a switch that generates a harmonically rich signal and then by selecting and transmitting one of the higher-frequency harmonics as the up-converted signal:

> Before setting the frequencies of the oscillating signals 5106 and 5112, the desired frequency of the transmitted signal must be determined. If it, too, is 900 MHz, then ***the frequency of the oscillating signal that causes the switch in the present invention to open and close must be a 'sub-harmonic' of 900 MHz***. That is, ***it must be the quotient of 900 MHz divided by an integer***. (In other words, 900 MHz must be a harmonic of the oscillating signal that drives the

switch.)

Id., 52:2-9; 61:42-62. It is this method of up-converting—using a control signal with a frequency that is a sub-harmonic and lower than the desired output frequency to generate the desired higher frequency harmonic—that provides the purported benefit of the invention. Specifically, it enables the claimed invention to up-convert using a low-frequency oscillator (which generates the low-frequency control signal) and thus avoids the use of higher cost, inefficient components. *Id.*, 9:56-58 ("Because it up-converts frequency, ***the present invention*** can take advantage of the relatively low cost of low frequency oscillators ….").

The claimed control signal must therefore be construed as "an oscillating signal that controls the first switch with a frequency that is a sub-harmonic of and lower than the desired output frequency." *Virnetx, Inc. v. Cisco Sys., Inc.*, 767 F.3d 1308, 1318 (Fed. Cir. 2014) (construing "secure communication link" to require anonymity where Summary of Invention touted the anonymity feature and this feature was "'repeatedly and consistently' used to characterize the invention" thus "strongly suggest[ing] that it should be read as part of the claim"); *Versata Software, Inc. v. SAP Am., Inc.*, 2009 WL 1408520, at *6 (E.D. Tex. May 19, 2009) (claim limited because "specification consistently describes 'this invention' as utilizing denormalized numbers" and "distinguishes the present invention over prior art precisely for the reason that the prior art did not use denormalized numbers").

PV's only criticism of Intel's "control signal" construction is that it refers to the "first switch." PV does not dispute that the control signal in claim 1 controls the recited "first switch," but PV notes that in unasserted claim 12, the control signal controls a switch identified as the "third switch." Pl. Op. 57. This argument misses the point. There is no dispute that, in the claimed invention, the control signal controls the switch that up-converts. In asserted claim 1, the up-converting switch is labeled the "first switch." In unasserted claim 12, the up-converting switch is labeled as the "third switch." But the claim

at issue is claim 1, and the "control signal" term in this claim refers to a signal that controls the "first switch." If claim 12 were at issue, the proposed construction of "control signal" for that claim would refer to the "third switch." PV's argument does not in any way alter that the control signal is the signal used to control the up-converting switch (described as the "first switch" in claim 1) and that it has a frequency that is a sub-harmonic of and lower than the desired output frequency.

PV's Proposal. PV's argument that "control signal" refers merely to a generic control signal—"a control signal is simply a signal that controls a switch" (Pl. Op. 57)—would read the invention out of the claim. The stated purpose of the claimed invention is to provide a purportedly new, cheaper method of up-conversion. '108, 9:56-58. As described above, the patent explains that it accomplishes this goal by using a particular type of "control signal"—one that will generate a harmonically rich signal that includes the desired harmonic that can be selected and used as the up-converted signal. *Id.*, Abstract, 2:4-41; 16:24-28. The desired harmonic—i.e., the desired up-converted signal—cannot be generated by just any control signal. It instead requires a control signal whose frequency is selected *based on* the desired frequency of the output signal—i.e. the control signal must be a subharmonic of and lower than the desired output frequency. *Id.,* 52:2-9 ("Before setting the frequencies of the oscillating signals 5106 and 5112, the desired frequency of the transmitted signal must be determined. If it, too, is 900 MHz, then ***the frequency of the oscillating signal that causes the switch in the present invention to open and close must be a 'sub-harmonic' of 900 MHz. That is, it must be the quotient of 900 MHz divided by an integer***. (In other words, 900 MHz must be a harmonic of the oscillating signal that drives the switch.)."), 61:42-62. To interpret the term otherwise would eliminate what PV claimed was the novel aspect of its purported invention.

PV's "plain meaning" construction is also improper because the parties have a clear dispute about the meaning of this term and that dispute should not be left to the jury to resolve. *O2 Micro Int'l*

Ltd. v. Beyond Innovation Tech. Co., 521 F.3d 1351, 1360 (Fed. Cir. 2008) ("When the parties raise an actual dispute regarding [claim scope], the court, not the jury, must resolve that dispute.")

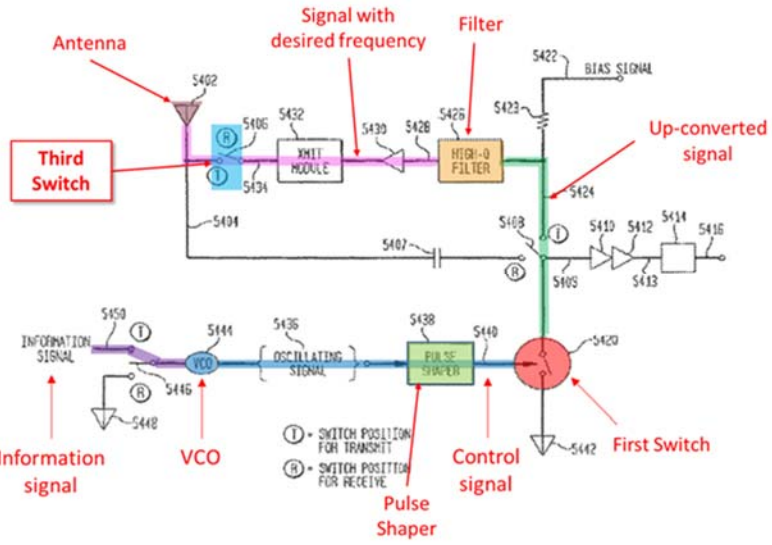
B. "third switch" ('108 patent, claim 1)

Proposed Constructions
Intel: "a switch controlling whether the antenna transmits said signal"
PV: Plain and ordinary meaning, or "switch" as construed by the Court in Case No. 6:20-cv-108

The parties dispute whether the "third switch" term should be construed consistent with its use in the '108 patent (as Intel proposes) or whether the term should be given a purported "plain and ordinary meaning" and can be applied to any switch in a circuit (as PV apparently proposes).

Intel's Proposal. Claim 1 of the '108 patent recites a "frequency conversion module" that includes three switches. The "first switch" is configured to "up-convert" a signal, and "said signal is transmitted by an antenna *connected to a third switch*." The patent explains that the third switch, by virtue of its connection to the antenna, controls whether the antenna transmits the upconverted signal.

The "third switch" is shown in Figure 54A below—which the patentee identified as supporting Claim 1 during the patent's prosecution—as "R/T switch 5406" (light blue). This switch connects to the antenna when a signal is to be transmitted.



'108, Fig. 54. As described above regarding the "control signal" term, and as shown in the figure, the "first switch" (red) performs up-conversion by generating a harmonically rich signal, and a filter (yellow) selects the higher-frequency harmonic signal that is to be transmitted via antenna 5402 (brown). The specification explains that the third switch (the switch connected to the antenna) then controls whether the antenna transmits the upconverted signal. Specifically, Figure 54A shows a "half duplex" system, which is a transceiver that can "either transmit or receive but cannot do both simultaneously." *Id.* 49:62-64. Because the antenna is used for both transmit and receive functions, the "R/T switch"—the third switch—controls whether the transceiver is in transmit mode or in receive mode. *Id.,* 55:46-48 ("A duplexer 5604 is used in the transceiver to permit the ***sharing of an antenna 5602 for both the transmit and receive functions***."). When the switch is closed, the transceiver is in transmit mode (shown as a "T" in the figure), and the signal to-be-transmitted flows through to the antenna. *Id.,* 55:5-25 ("***When the transceiver is performing the transmit function, the R/T switches 5406, 5408, and 5446/5452 (FM or PM) are in the (T) position.*** … Again, because the transceiver is performing the transmit function, ***R/T switch 5406 connects the transmission signal to the antenna 5402***."). When the switch is open, the transceiver is in receive mode, and the signal is blocked from flowing through to the antenna. *Id.*, 54:39-43. Thus, the "R/T switch 5406"—i.e. the "third switch" described in Claim 1—controls whether the signal is transmitted. *Id.,* 54:30-58. The third switch is therefore properly construed as a switch controlling whether the antenna transmits said signal.

PV argues that Intel's construction improperly "require[s] a special purpose (controlling an antenna) for the third switch." Pl. Op. 58. But as explained above, the only disclosed switch corresponding to the "third switch" performs precisely that function. The Federal Circuit has found it "entirely proper to consider the functions of an invention in seeking to determine the meaning of particular claim language." *Medrad, Inc. v. MRI Devices Corp.*, 401 F.3d 1313, 1318-19 (Fed. Cir.

2005) (incorporating function—taking MRI images—in construing term "substantially uniform magnetic field" to mean "substantially uniform to obtain useful MRI images").[25]

PV's Proposal. PV's proposal that the "third switch" should be given its purported plain and ordinary meaning amounts to an assertion that ***any*** switch in the transceiver that is connected even indirectly to the antenna—including through multiple other components—could constitute the required third switch. Such a reading would render the "third switch" claim language meaningless since ***every*** component in a circuit is arguably connected to every other component in the circuit through intermediate components. Indeed, PV's interpretation would improperly eliminate any distinction between the "third switch" and the claimed "first" and "second" switches. *Engel Indus. v. Lockformer Co.*, 96 F.3d 1398, 1404-05 (Fed. Cir. 1996) (where claim required two separate elements, "second portion" and "return portion," two elements "logically cannot be one and the same").

C. "pulse shaper" ('108 patent, claims 6, 8)

Proposed Constructions
Intel: "a circuit configured to enhance a desired harmonic by shaping an oscillating signal" **PV**: "circuitry that generates a string of pulses"

The parties dispute whether the term "pulse shaper" should be construed in accordance with the definition provided in the specification (as Intel proposes) or whether an alternative construction should be adopted (as PV proposes).

Intel's Proposal. Intel's proposed construction expressly tracks the definition in the patent. The patent equates pulse shaping with "harmonic enhancement." *Id.*, 42:21-22 ("Harmonic

[25] PV argues that Intel's construction is incorrect because in nonasserted claim 12, the roles of the "first switch" and "third switch" are reversed. But as explained above, the construction must be read within the context of the relevant claim—asserted claim 1—where it is the "third switch" that controls whether the system transmits the signal. If claim 12 were at issue, the "first switch" would be understood to control whether the system transmits the signal.

enhancement may also be called 'pulse shaping' ….''). And the patent defines the "pulse shaper" as a "harmonic enhancement module." *Id.*, 42:49-50 ("The harmonic enhancement module (HEM) 4602 (Fig. 46) is also referred to as a 'pulse shaper.'").

The '108 patent explains that the goal of pulse shaping or harmonic enhancement is to help create the "harmonically rich" signal that is critical to the patent's method of up-conversion. Figure 28A shows a switch module 1214 that is used to convert a modulated oscillating signal 2804 into harmonically rich signal 2814. Switch module 1214 could be used, for example, as switch 5420 in the embodiment of Figure 54A. The patent explains that to generate the harmonically rich signal, "the switch 2816 preferably closes and opens crisply," *id.*, 41:41-43, and for "[f]or the switch 2816 to close and open crisply, the oscillating signal 2804, [that controls the switch,] must also be crisp," *id.*, 41:51-52. The pulse shaper precedes the switch (*see* pulse shaper 5438 in Figure 54A) and makes the input oscillating signal 2804 into a crisp, rectangular waveform:

> If the oscillating signal is sinusoidal, ***harmonic enhancement will shape the sinusoidal signal*** into a rectangular (or substantially rectangular) waveform with the desired pulse width to period ratio. If the oscillating signal 2804 is already a square wave or a pulse, ***harmonic enhancement will shape it*** to achieve the desired ratio of pulse width to period.

Id., 42:19-29, Fig. 39-42, 43:38-45:67. The output of the pulse shaper is then applied to the switch 2816, thereby controlling when and how the switch is open and closed. By modifying the shape of the oscillating signal (e.g., squaring off the sine waves, narrowing the pulses, etc.), the pulse shaper enhances the harmonics and ensures that the switch generates the proper harmonically rich signal. '108, 43:17-26. Consistent with Intel's proposed construction, a pulse shaper is, thus, "a circuit configured to enhance a desired harmonic by shaping an oscillating signal."

PV's Proposal. PV proposes construing "pulse shaper" to mean "circuitry that generates a string of pulses"—meaning that ***any*** circuitry that generates a string of pulses would constitute a "pulse shaper." But that construction ignores the definitional statements in the patent and effectively reads the

word "shaper" out of the claim, replacing it with the word "generator." Indeed, under PV's construction, even circuitry that *reduces* a desired harmonic, as long as it outputs a string of pulses, would constitute a "pulse shaper." But weakening the desired harmonic is contrary to the entire purpose of the invention, which is to up-convert by generating a desired harmonic. Moreover, even a switch would arguably constitute a "pulse shaper," since the patent makes clear that the relevant switch in the patent generates a harmonically rich signal that constitutes a string of pulses. *Id.*, 19:27-30, 32:8-11, 61:54-56. Yet the specification describes, and the figures show, the pulse shaper as distinct from a switch. *Id.*, 42:19-31, 42:49-64; Fig. 54 (showing pulse shaper 5438 as separate from switch 5420).

PV's only purported support for its proposal is language in the specification stating that the output of the pulse shaper will be "a string of pulses." Pl. Op. 59. It is undisputed that a pulse shaper will output "a string of pulses." But just as it would be improper to construe a "boat" as merely "a vehicle," it is insufficient to construe "pulse shaper" without the elements that distinguish it from all other devices—such as switches—that can "generate a string of pulses." Indeed, the patent makes clear that pulse shapers do not merely generate pulses but create a particular type of string of pulses—i.e., pulses of a desired width—in order to enhance a desired harmonic. *Id.*, 42:21-23 ("Harmonic enhancement may also be called 'pulse shaping' since the purpose is to shape the oscillating signal 2804 into a string of pulses ***of a desired pulse width***."), 41:4-8 ("[P]ulse width is an important factor in assuring that the harmonic waveform at the desired output frequency has sufficient amplitude to be useful without requiring elaborate filtering or unnecessary amplification."). PV's proposed construction is inconsistent with the intrinsic evidence and should therefore be rejected.

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Respectfully submitted,

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CERTIFICATE OF SERVICE

I hereby certify that all counsel of record who are deemed to have consented to electronic service are being served with a copy of the foregoing document via the Court's CM/ECF system per Local Civil Rule CV-5(b)(1) on April 2, 2021.

/s/ J. Stephen Ravel
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